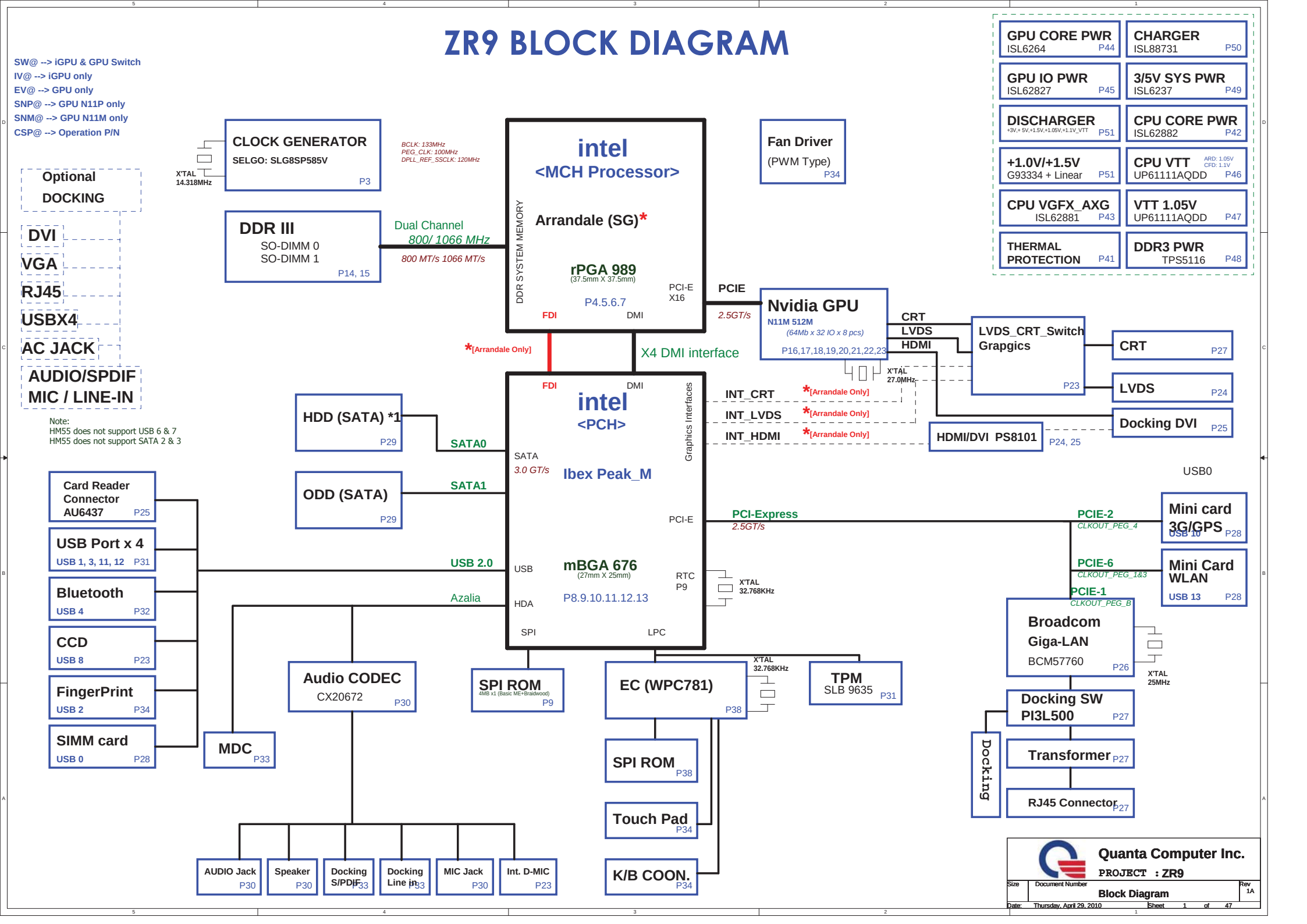
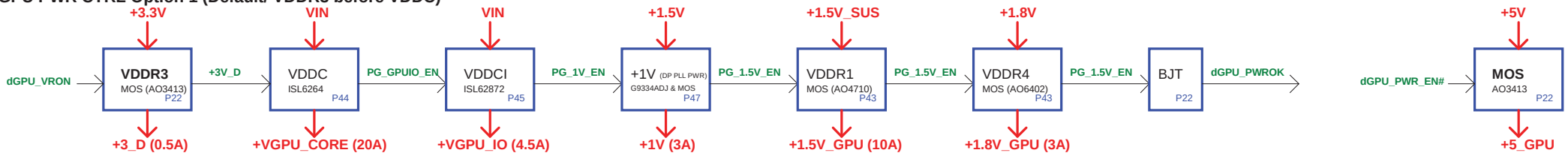
ZR9 BLOCK DIAGRAM

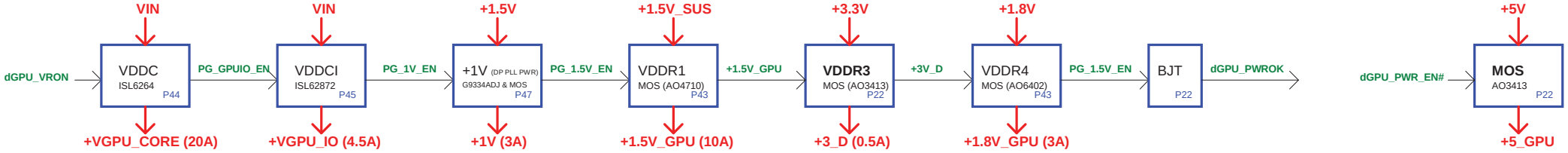
SW@ --> iGPU & GPU Switch
IV@ --> iGPU only
EV@ --> GPU only
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only
CSP@ --> Operation P/N



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



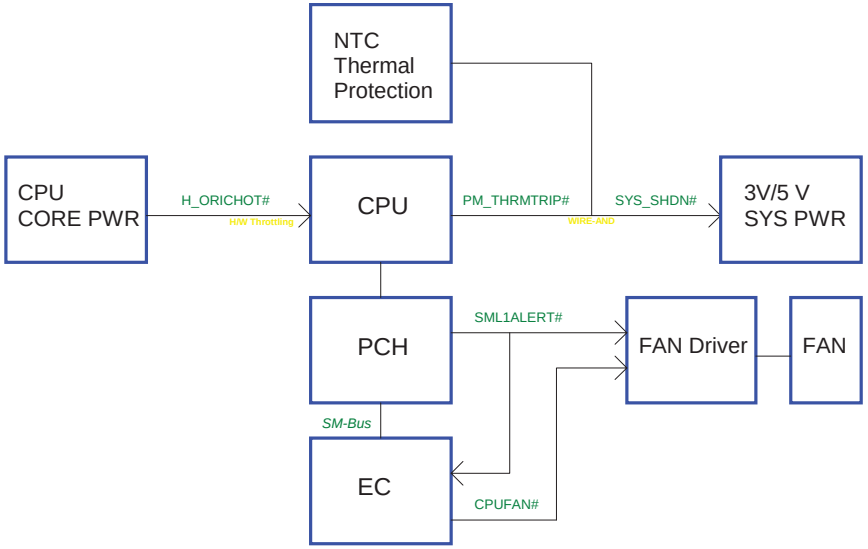
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

Thermal Follow Chart

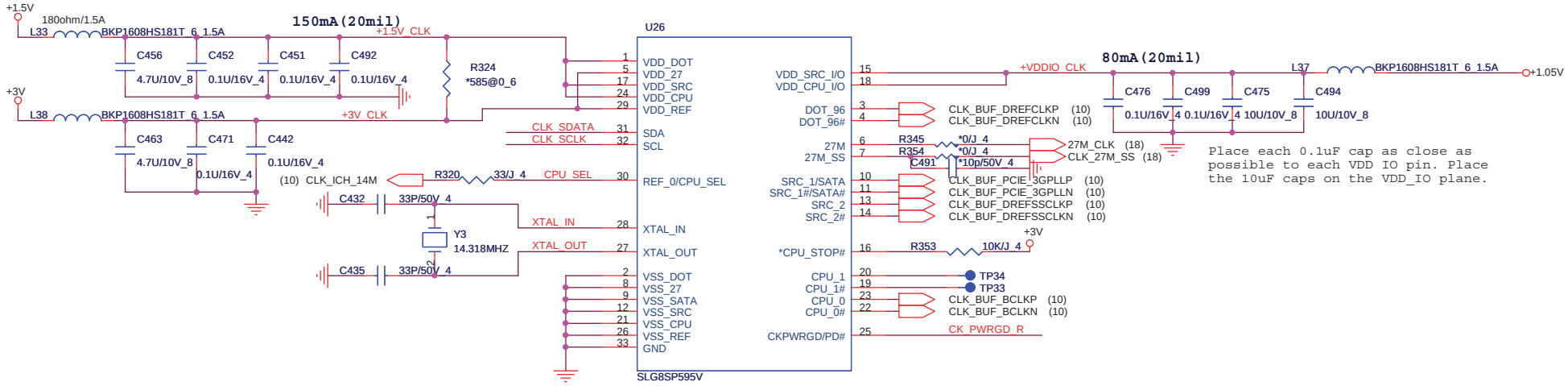


Quanta Computer Inc.

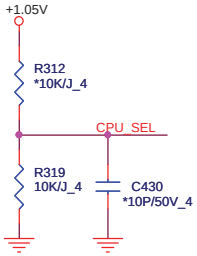
PROJECT : ZR9

Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

Date: Thursday, April 29, 2010 Sheet 2 of 47

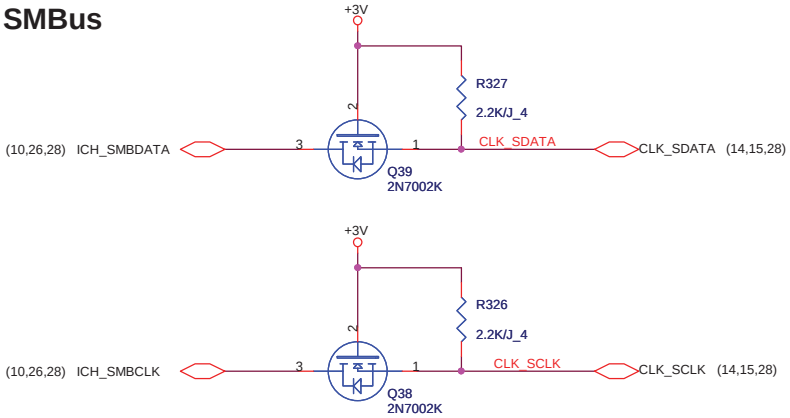


CPU_CLK select

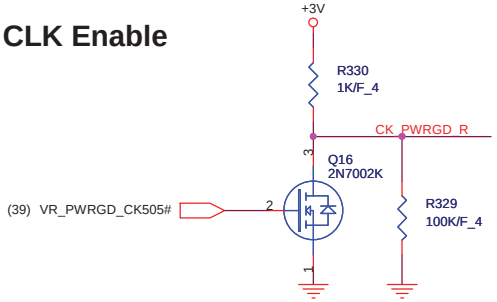


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



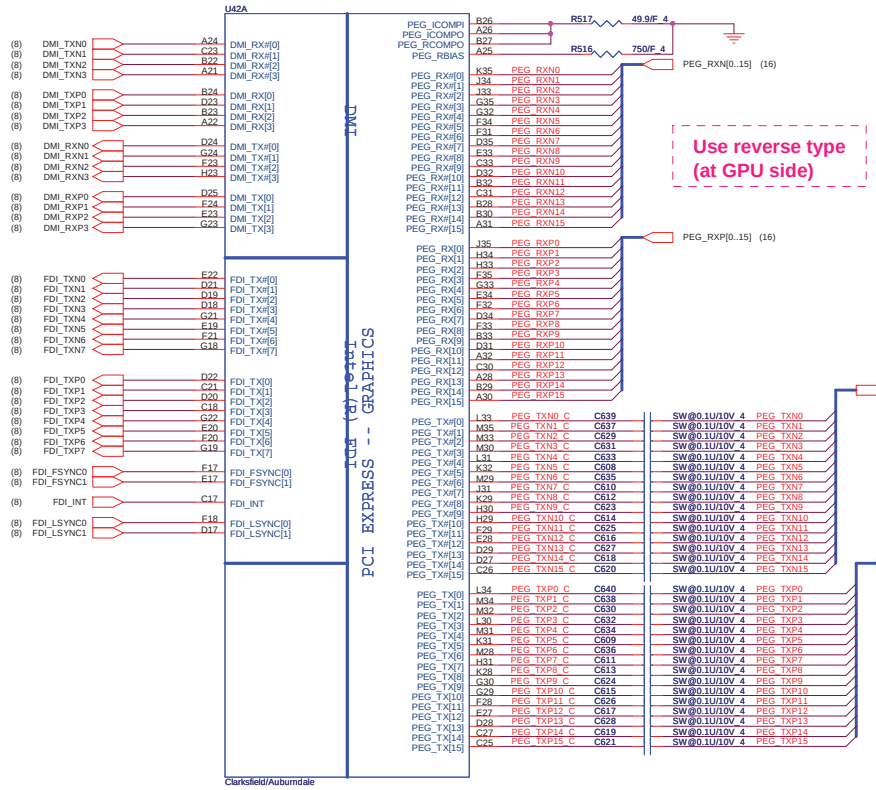
Quanta Computer Inc.

PROJECT : ZR9

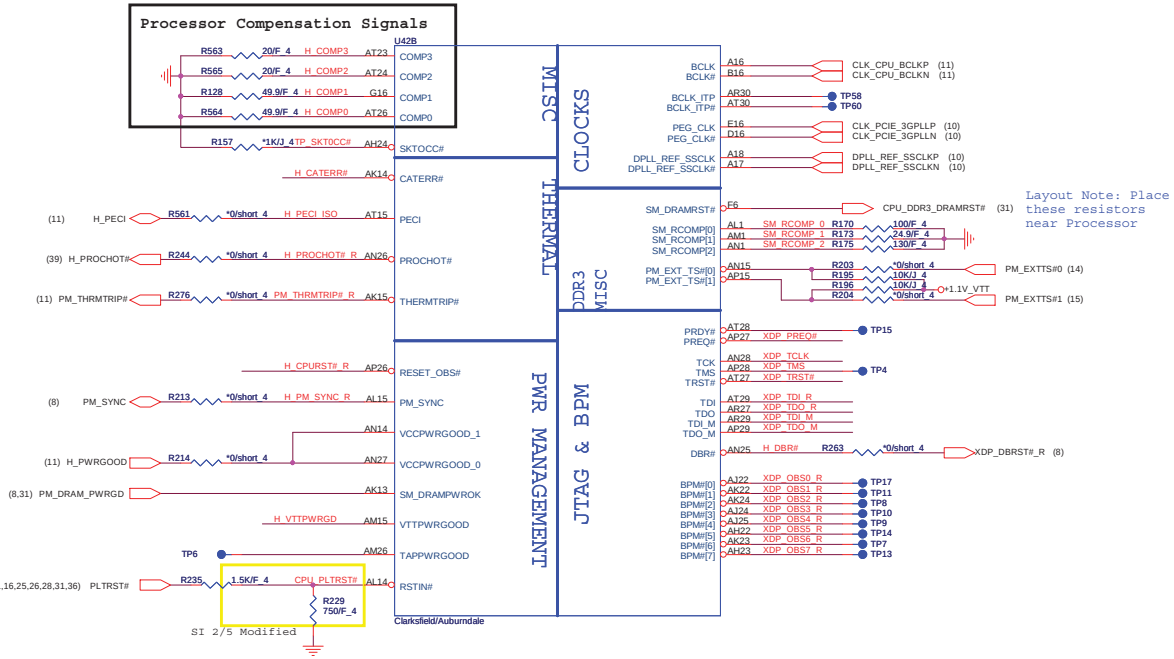
Size	Document Number	Rev
	Clock Generator	1A

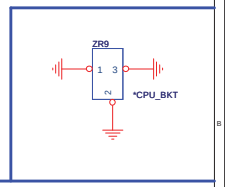
Date: Thursday, May 06, 2010 Sheet 3 of 47

AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

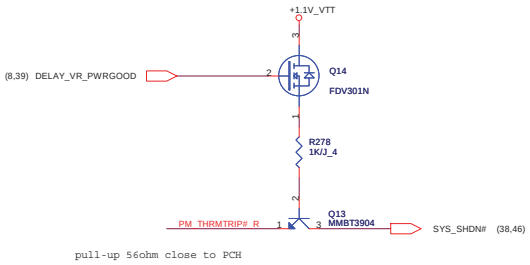


AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

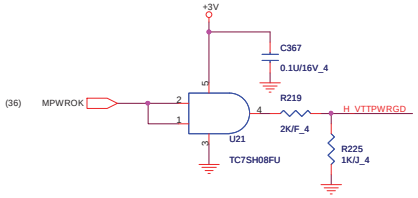




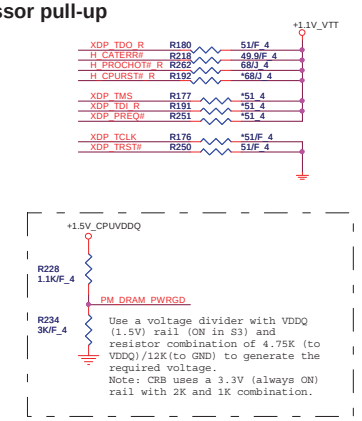
Thermaltrip protect



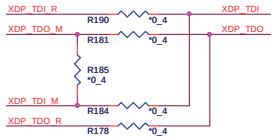
VTT PWR_Good



Processor pull-up



JTAG MAPPING



Scan Chain (Default)	STUFF -> R535, R538, R528 NO STUFF -> R536, R534
CPU Only	STUFF -> R536, R534 NO STUFF -> R535, R538, R528
GMCH Only	STUFF -> R534, R528 NO STUFF -> R538, R536, R535

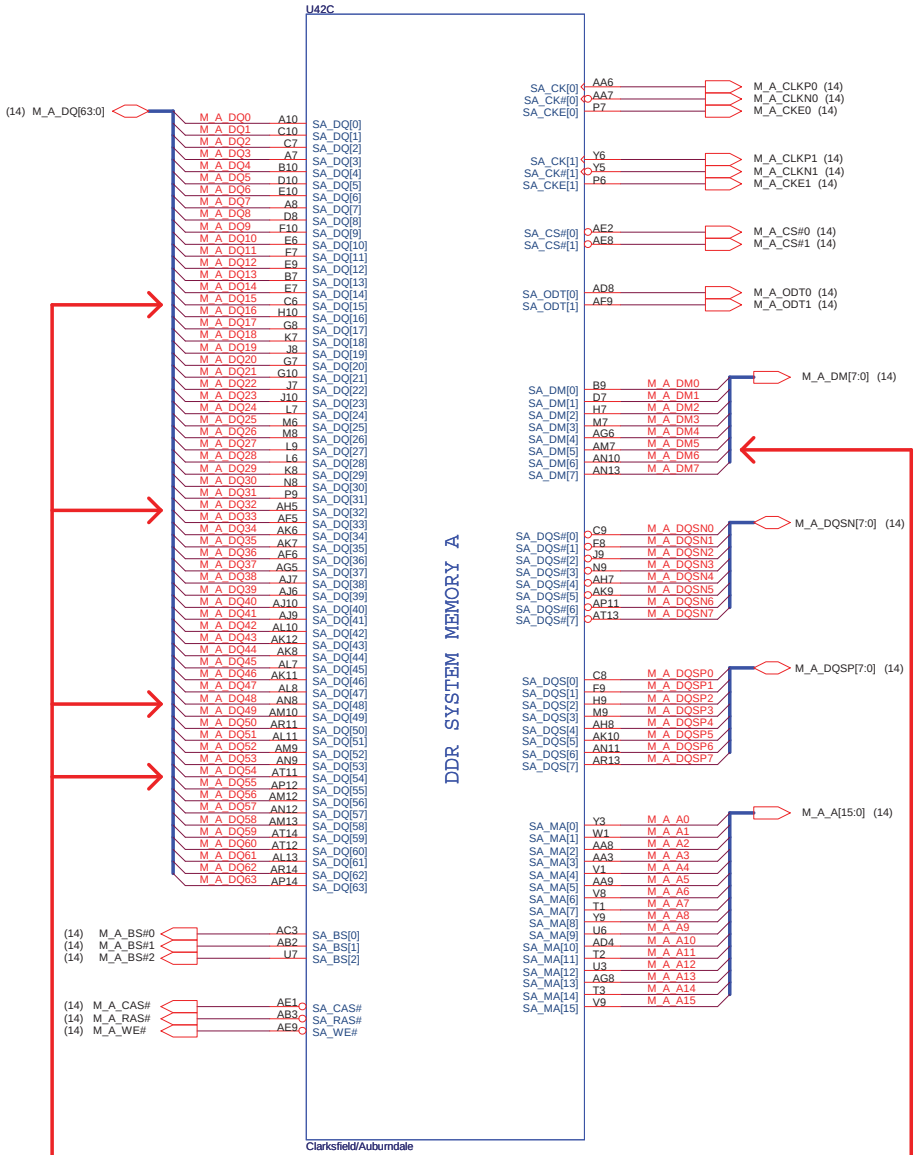
Quanta Computer Inc.

PROJECT : ZR9

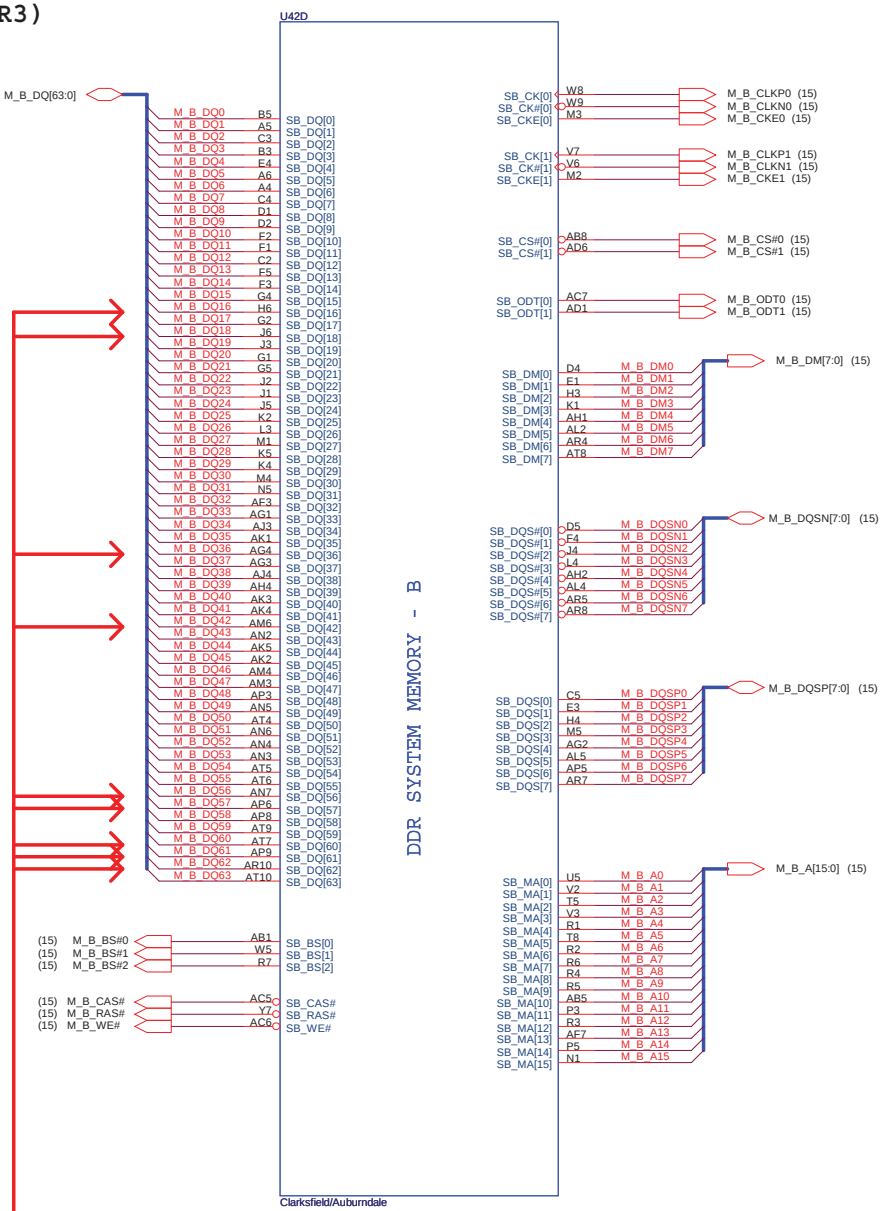
Size	Document Number	Rev
	AUBURNDA 1/4	1A

Date: Thursday, May 06, 2010 Sheet 4 of 47

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.



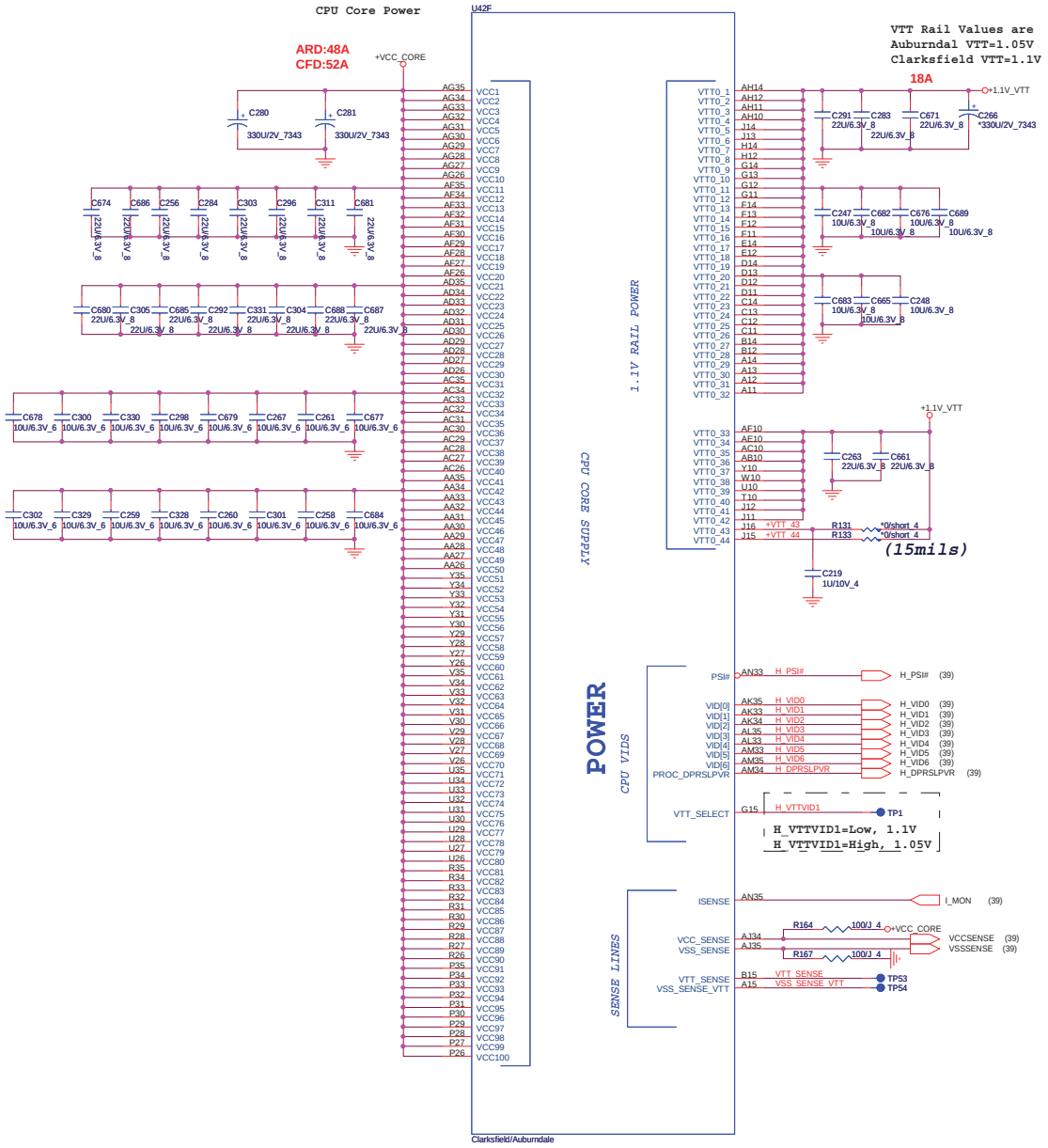
Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

Quanta Computer Inc.

PROJECT : ZR9

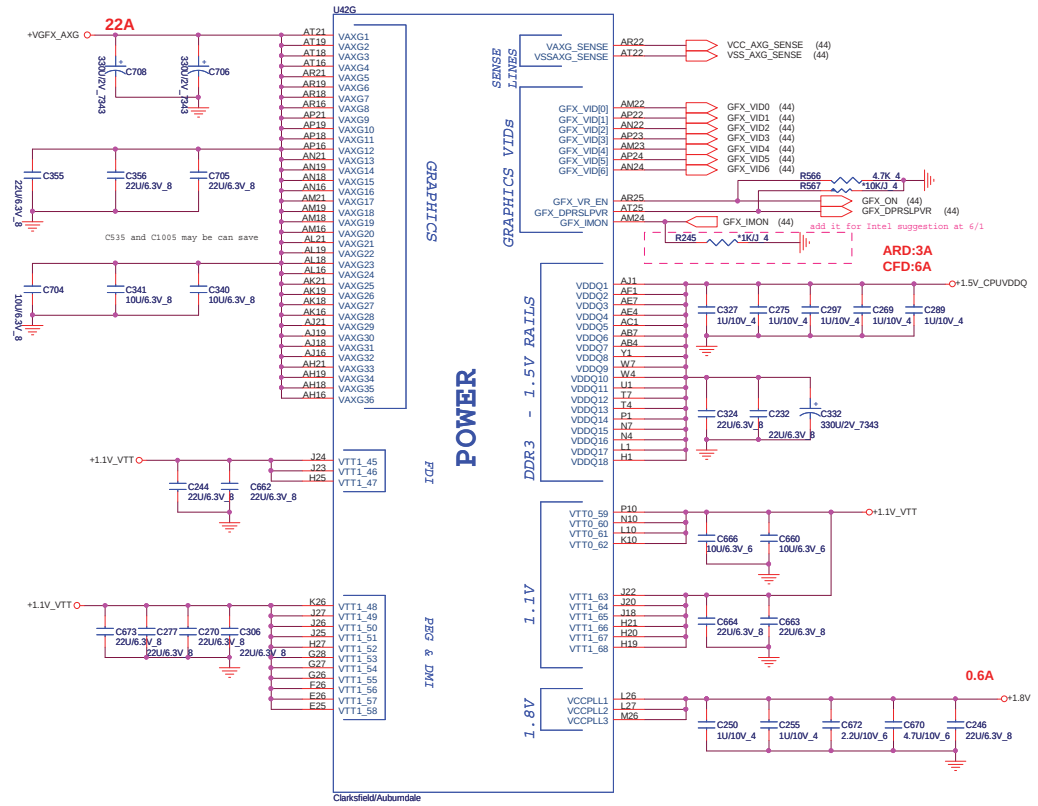
Size	Document Number	Rev
	AUBURNDA 2/4	1A

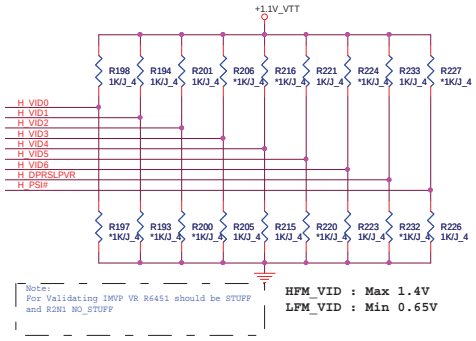
Date: Wednesday, May 05, 2010 Sheet 5 of 47



AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)





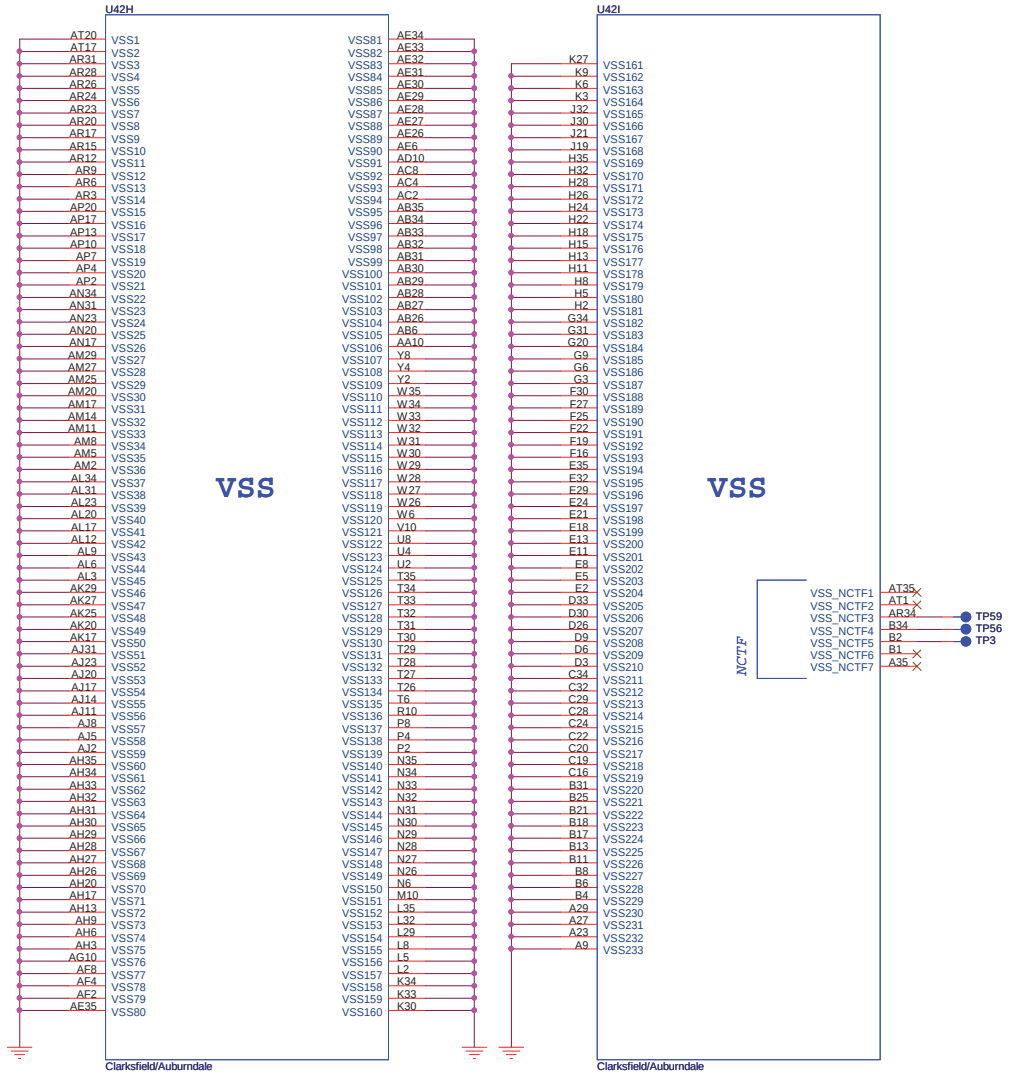
Quanta Computer Inc.

PROJECT : ZR9

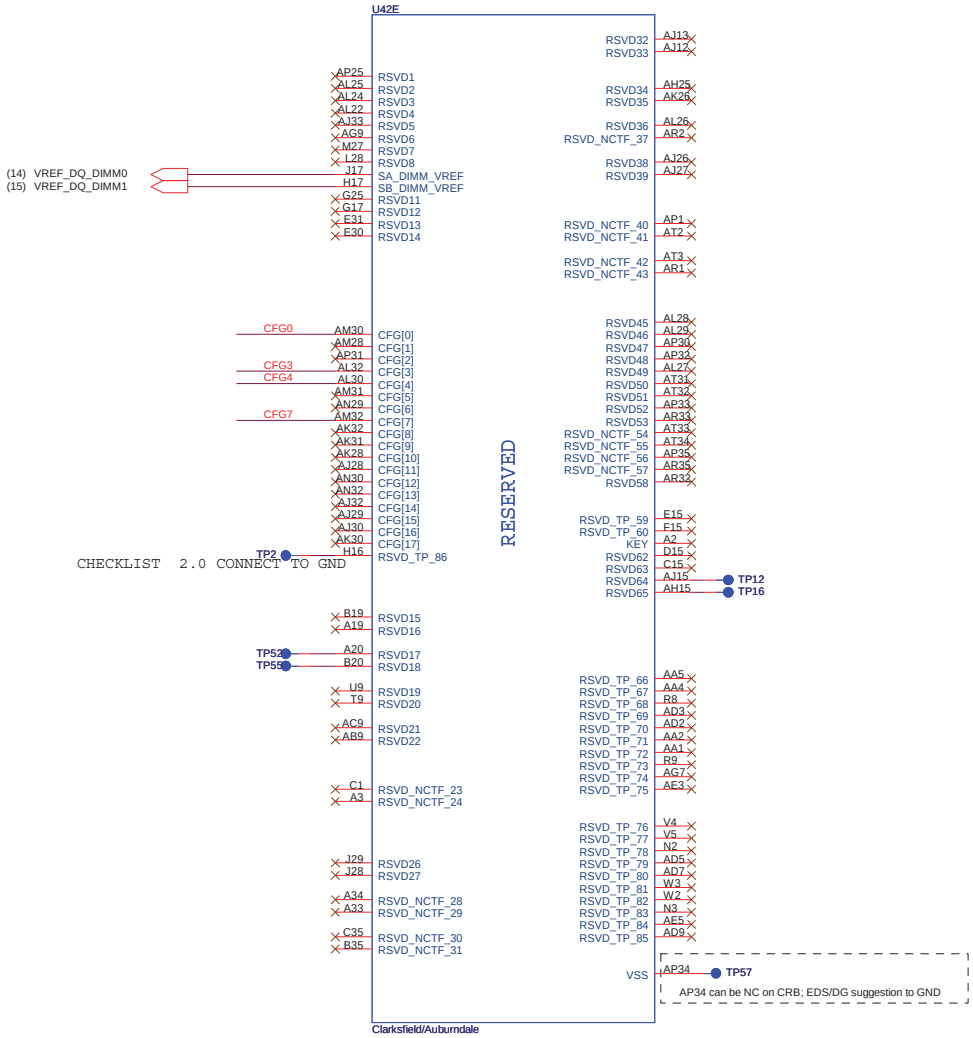
Size	Document Number	Rev
	AUBURNDA 3/4 (PWR)	1A

Date: Thursday, May 06, 2010 Sheet 6 of 47

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



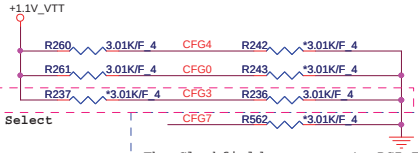
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG



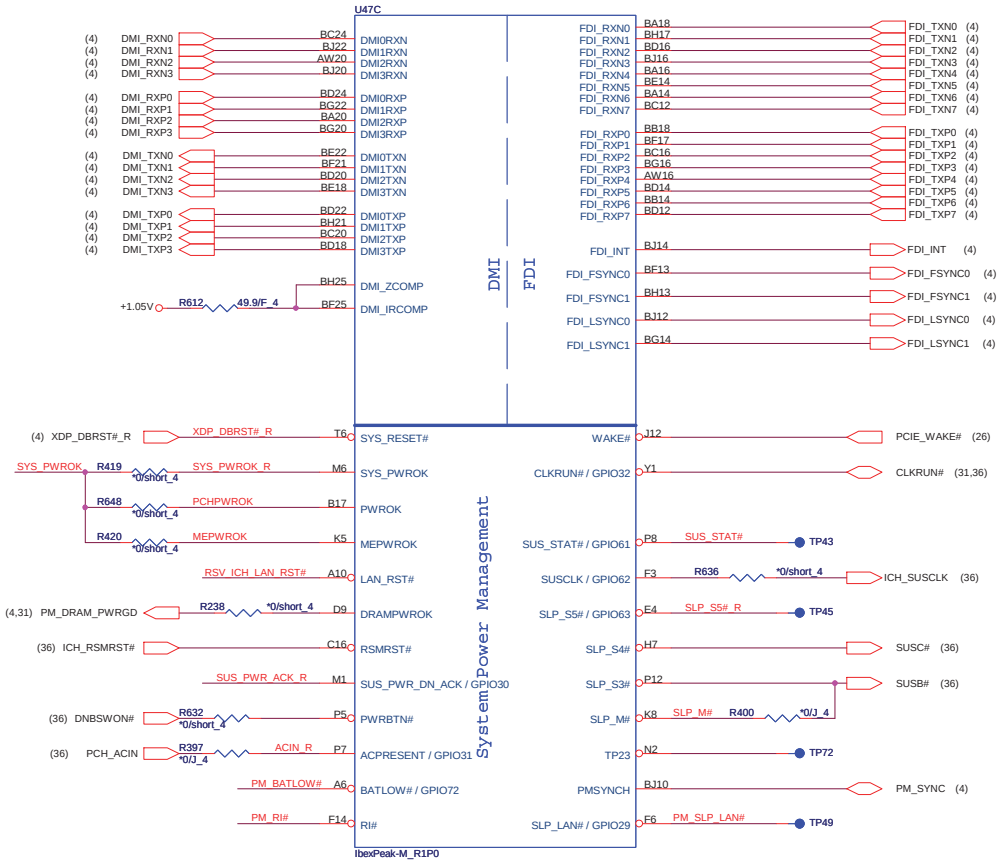
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

Quanta Computer Inc.
PROJECT : ZR9

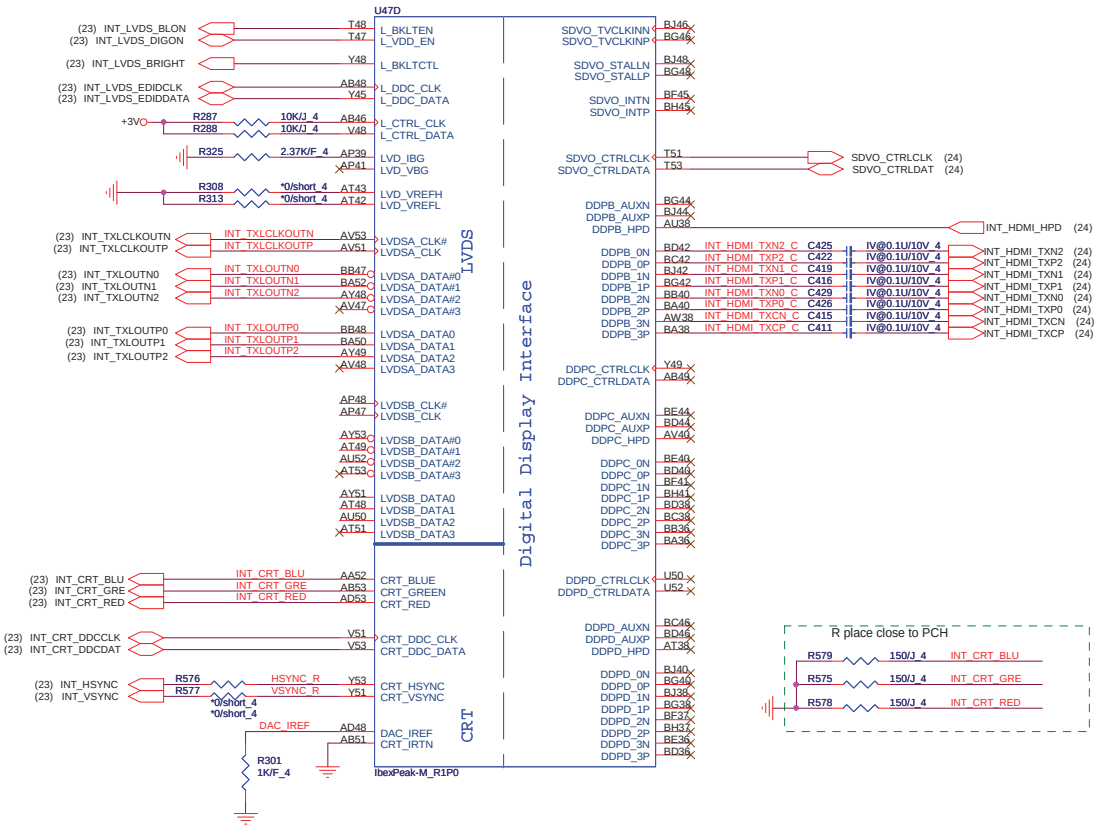
Size	Document Number	Rev
	AUBURNDA 4/4	1A

Date: Wednesday, May 05, 2010 Sheet 7 of 47

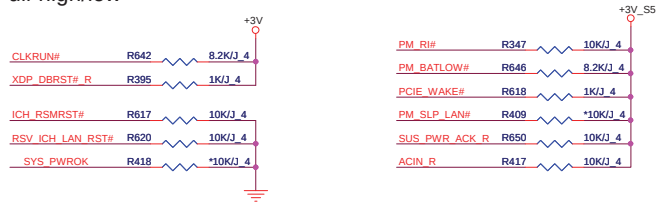
IBEX PEAK-M (DMI,FDI,GPIO)



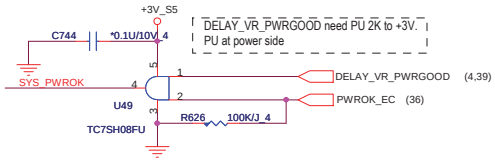
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



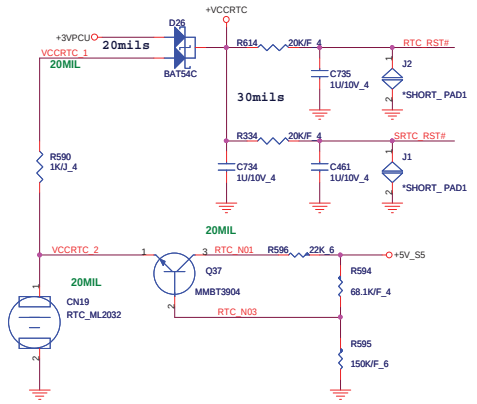
Quanta Computer Inc.

PROJECT : ZR9

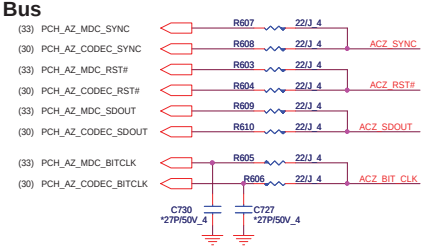
Size	Document Number	Rev
	IBEX PEAK-M 1/6	1A

Date: Thursday, May 06, 2010 Sheet 8 of 47

RTC Circuitry

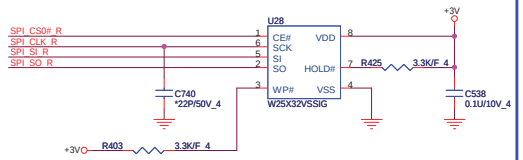


HDA Bus

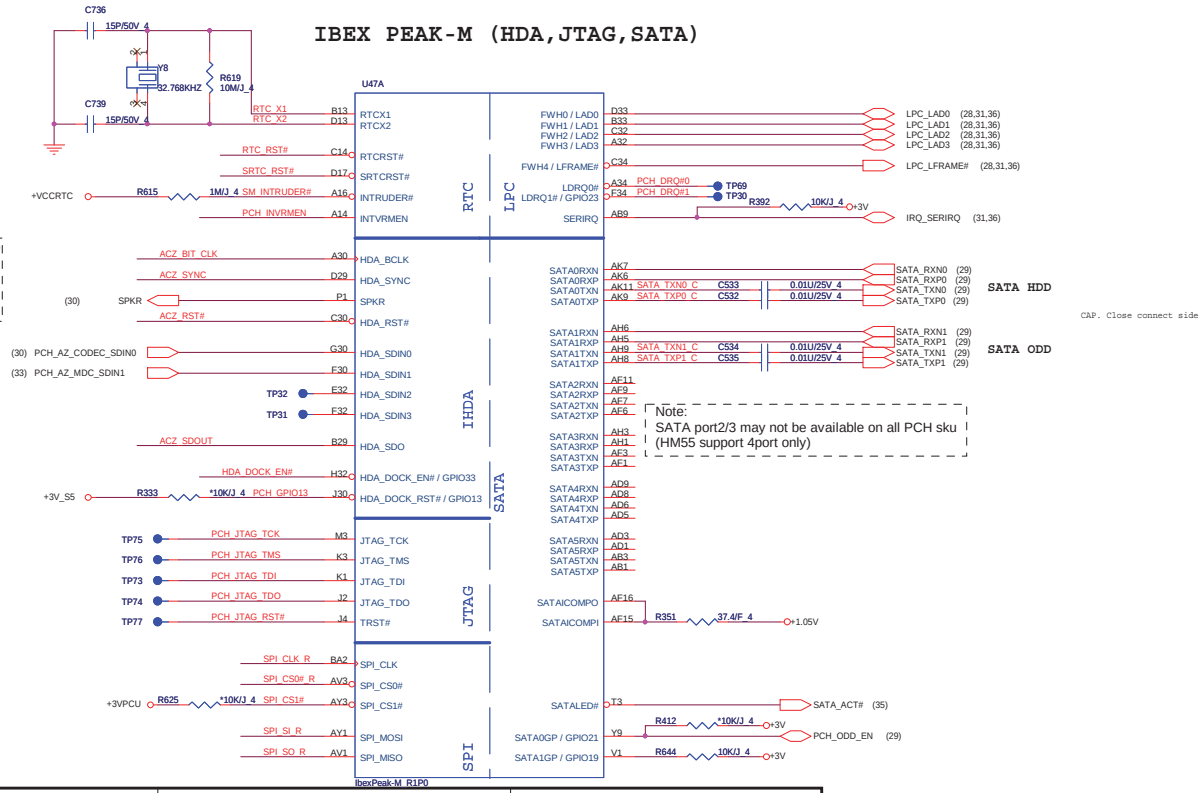


Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI



IBEX PEAK-M (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R633 *10K/J_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R583 *4.7K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC R616 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] +3V R286 *1K/J_4 R282 *1K/J_4 R285 1K/J_4 R306 1K/J_4 PCI_GNT0# (10) PCI_GNT1# (10)
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	R307 *4.7K_4 PWM_SELECT# (10,23)
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R623 *1K/J_4 NV_ALE NV_ALE (10)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R622 *1K/J_4 NV_CLE NV_CLE (10)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R310 *1K/J_4 R309 *10K/J_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R624 *1K/J_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R383 10K/J_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	R364 *10K/J_4 RSV_GPIO27 (11)
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R414 1K/J_4 CR_WAKE# (11)

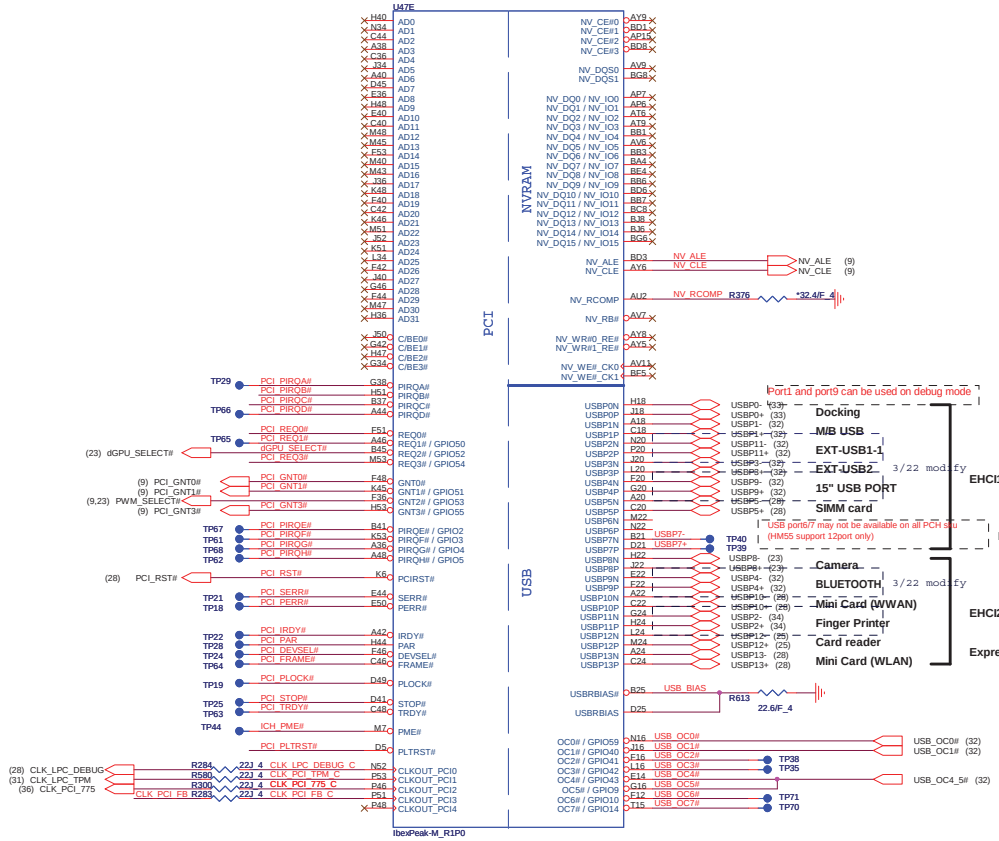
Quanta Computer Inc.

PROJECT : ZR9

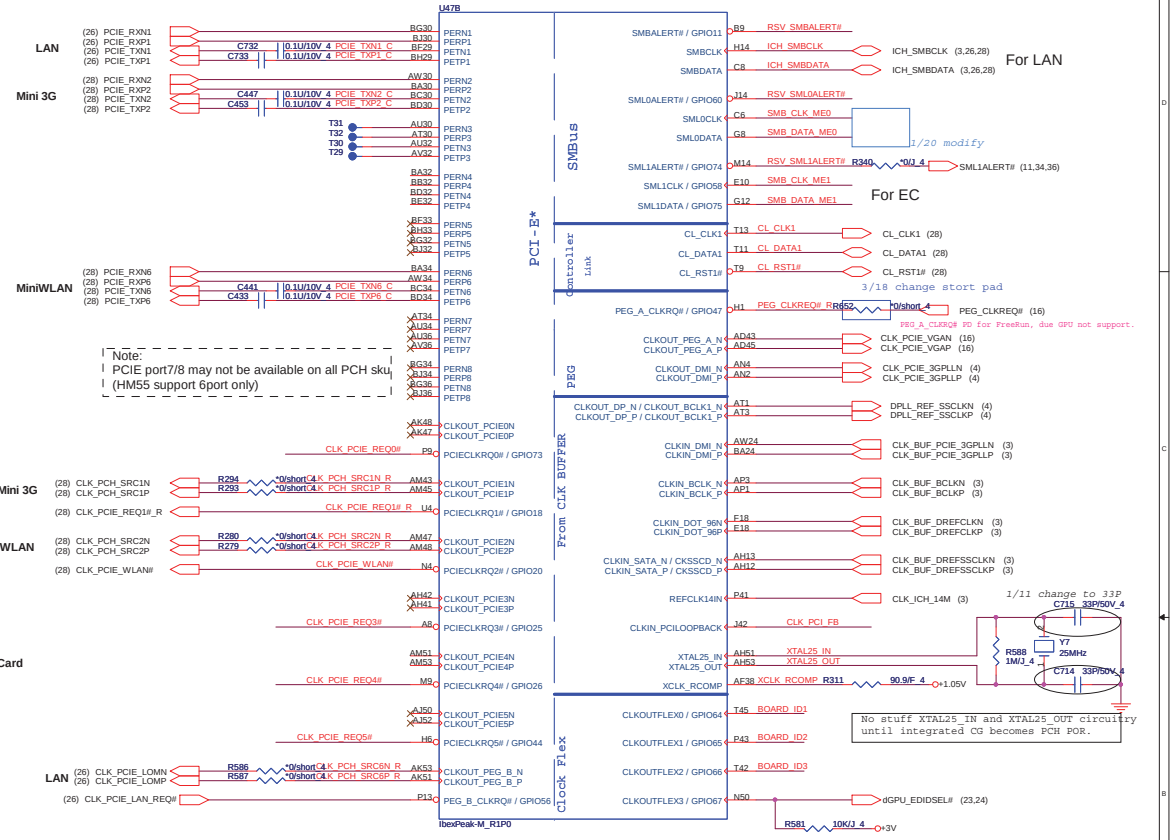
Size	Document Number	Rev
	IBEX PEAK-M 2/6	1A

Date: Wednesday, May 05, 2010 Sheet 9 of 47

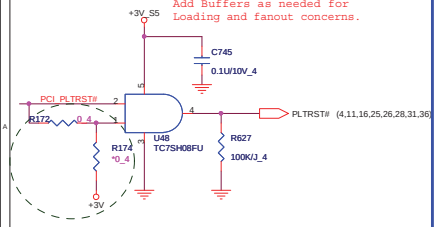
IBEX PEAK-M (PCI,USB,NVRAM)



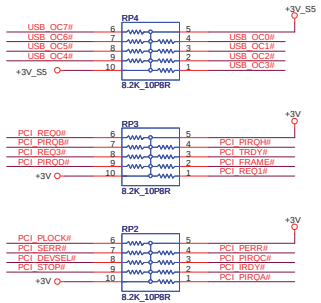
IBEX PEAK-M (PCI-E,SMBUS,CLK)



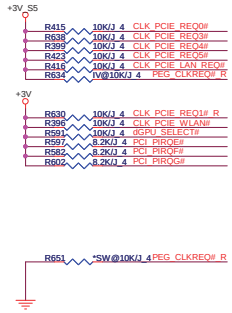
PLTRST#



PCI/USBOC# Pull-up



CLK_REQ/Strap Pin



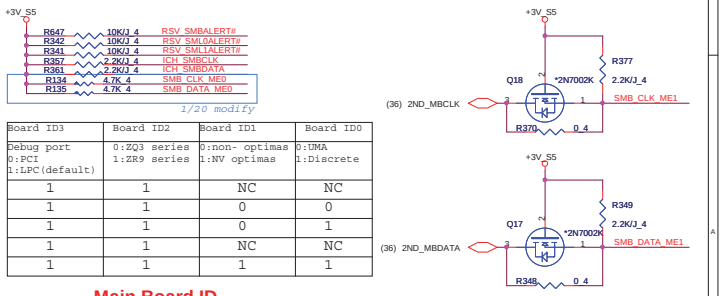
PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

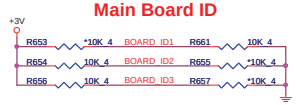
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

SMBus/Pull-up



Board ID3	Board ID2	Board ID1	Board ID0
Debug port 0:PCI 1:LPC(default)	0:ZQ3 series 1:ZR9 series	0:non- optimas 1:NV optimas	0:UMA 1:Discrete
1	1	NC	NC
1	1	0	0
1	1	0	1
1	1	NC	NC
1	1	1	1

Main Board ID



Quanta Computer Inc.

PROJECT ZR9

Size	Document Number	Rev
	IBEX PEAK-M 3/6	1A

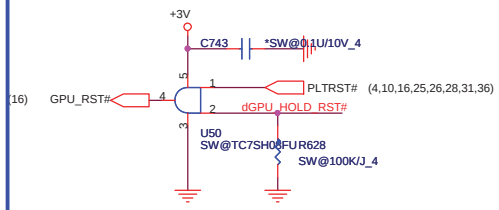
Date: Wednesday, May 05, 2010 Sheet 10 of 47

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

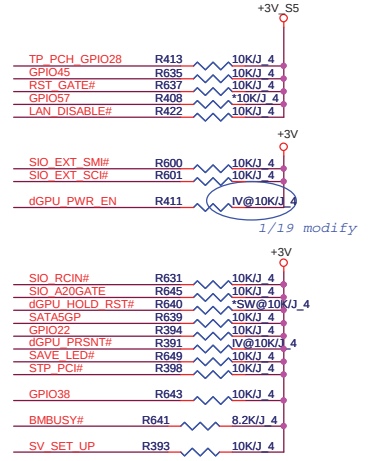
EC suggestion use GPIO49 for FAN control

SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

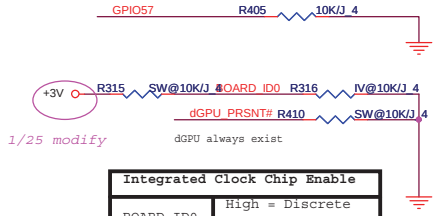
GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)



Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

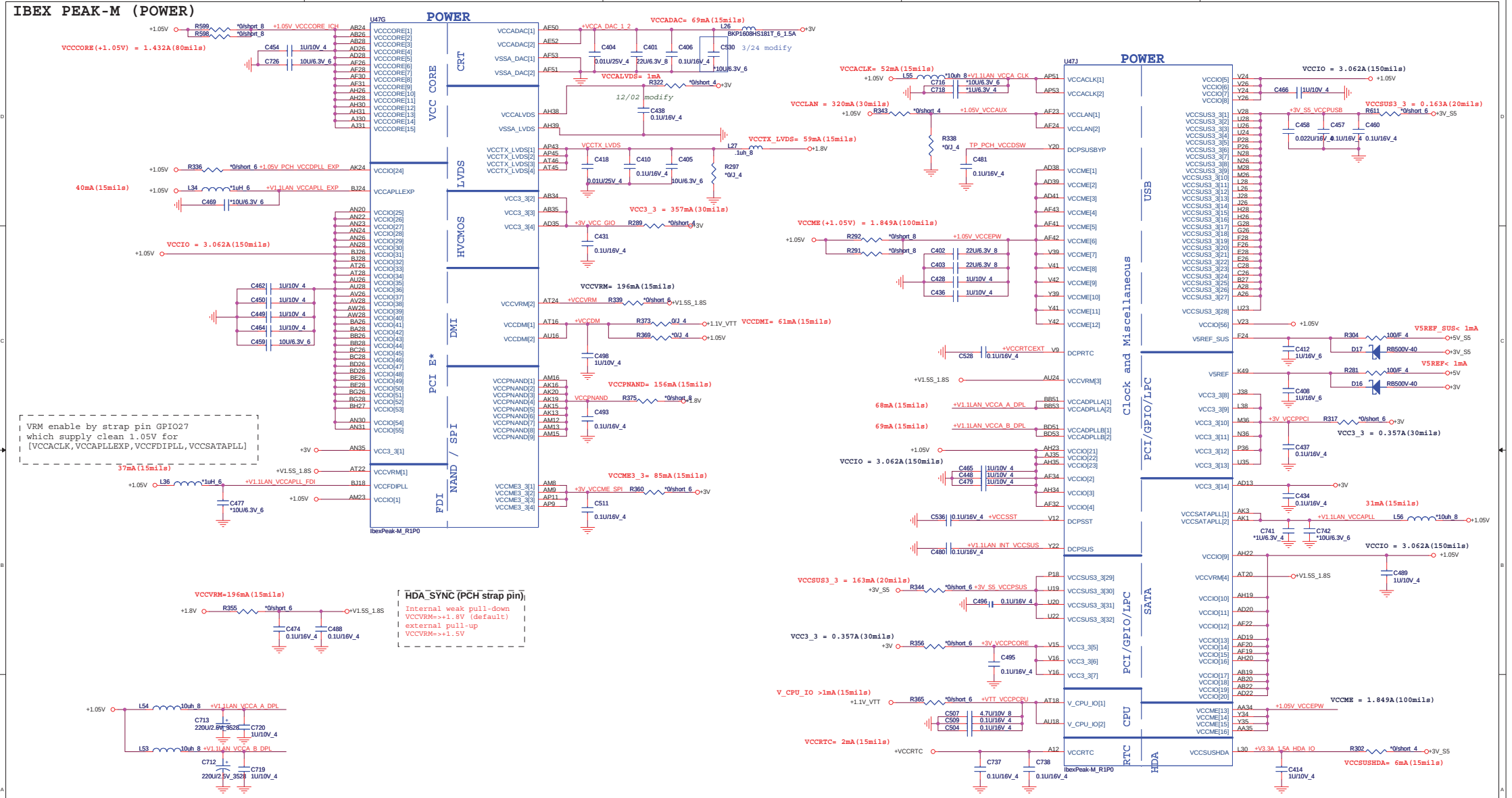
Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	IBEX PEAK-M 4/6	1A

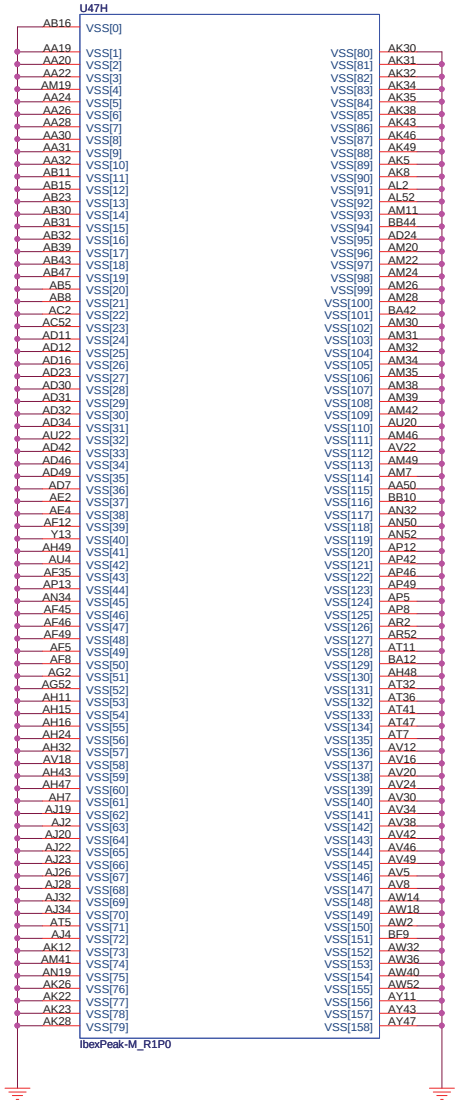
Date: Wednesday, May 05, 2010 Sheet 11 of 47

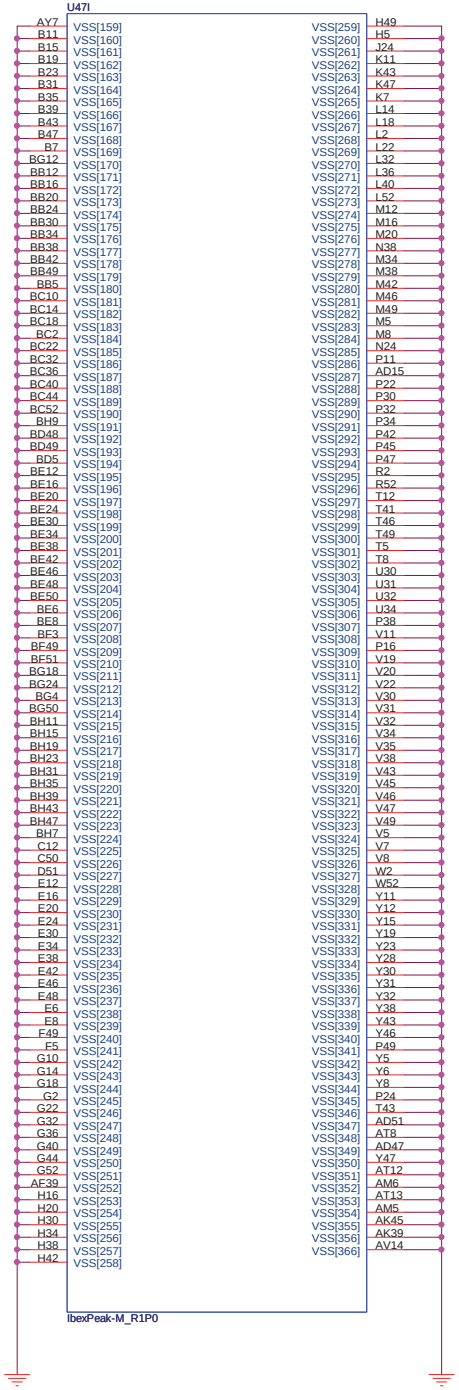
IBEX PEAK-M (POWER)



Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: IBEX PEAK-M 5/6	Rev 1A
Date: Thursday, April 29, 2010	Sheet 12 of 47	

IBEX PEAK-M (GND)



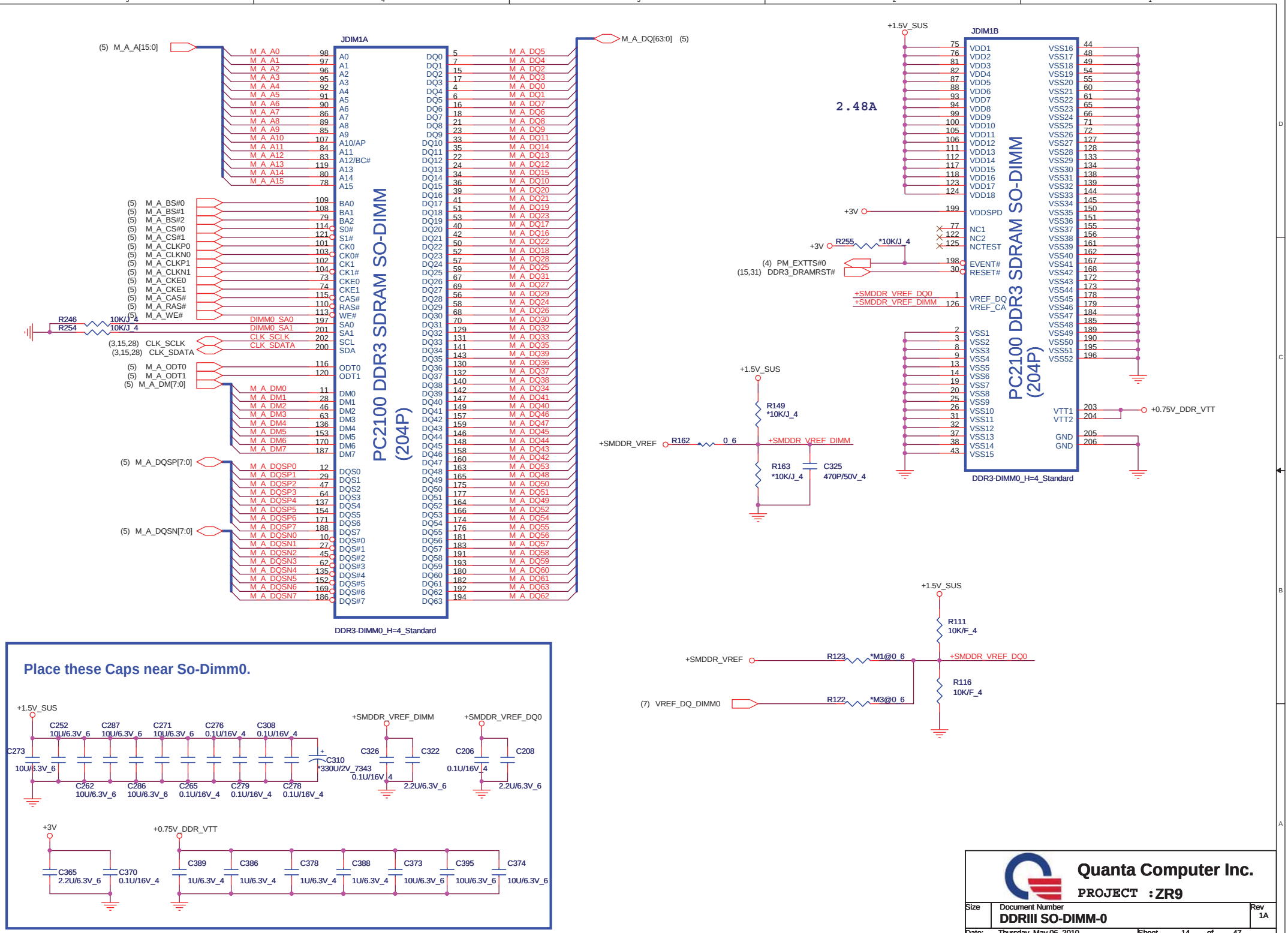


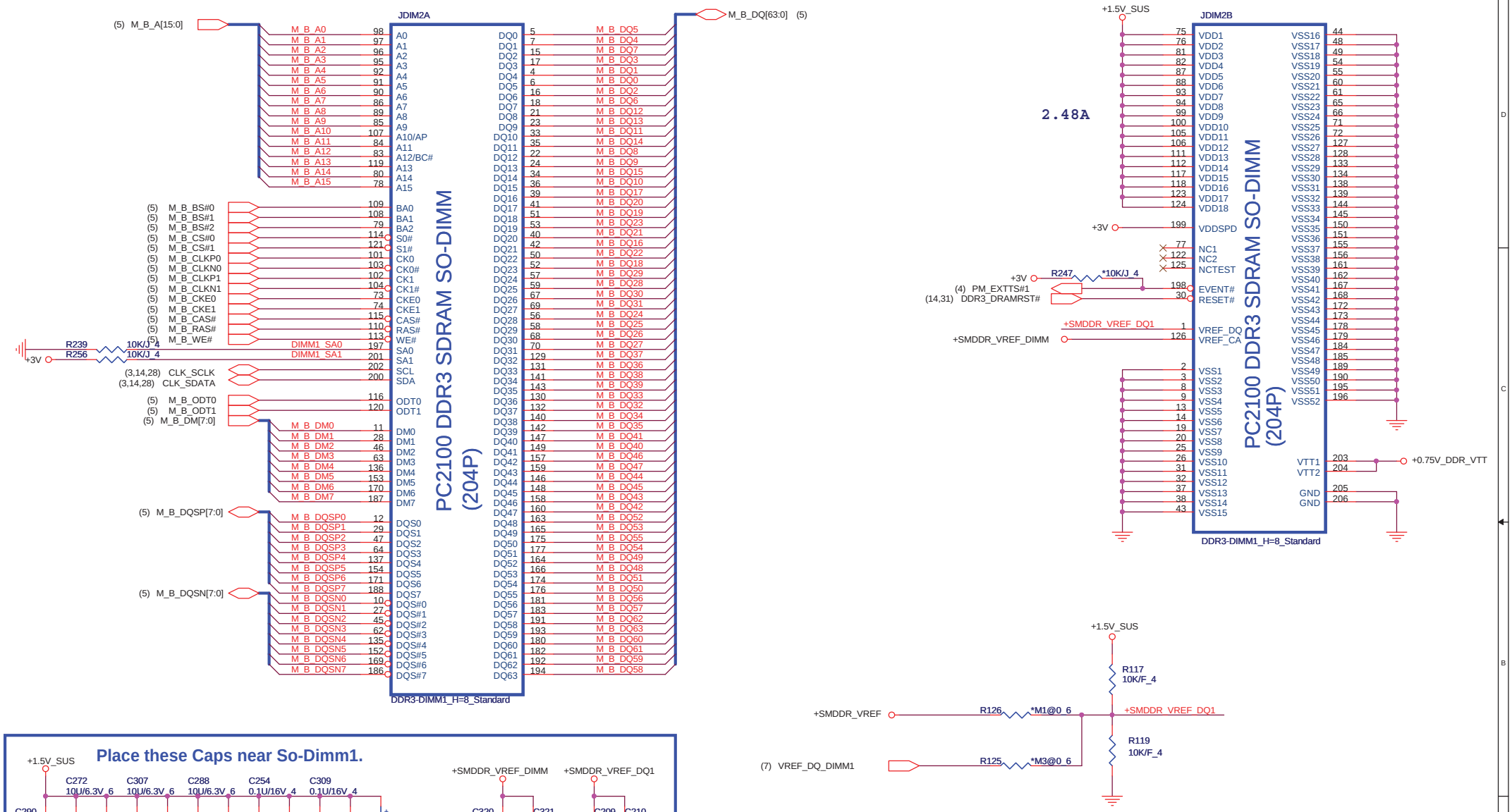
Quanta Computer Inc.

PROJECT :ZR9

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

Date: Thursday, April 29, 2010 Sheet 13 of 47


JDIM1A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM0_H=4_Standard
(5) M_A_A[15:0]
M_A_DQ[63:0] (5)
(5) M_A_BS#0
(5) M_A_BS#1
(5) M_A_BS#2
(5) M_A_CS#0
(5) M_A_CS#1
(5) M_A_CLKP0
(5) M_A_CLKN0
(5) M_A_CLKP1
(5) M_A_CLKN1
(5) M_A_CKE0
(5) M_A_CKE1
(5) M_A_CAS#
(5) M_A_RAS#
(5) M_A_WE#
R246 10K/J_4
R254 10K/J_4
DIMM0_SA0
DIMM0_SA1
(3,15,28) CLK_SCLK
(3,15,28) CLK_SDATA
(5) M_A_ODT0
(5) M_A_ODT1
(5) M_A_DM[7:0]
(5) M_A_DQSP[7:0]
(5) M_A_DQSN[7:0]
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM0_H=4_Standard
+1.5V_SUS
2.48A
+3V
R255 *10K/J_4
(4) PM_EXTTS#0
(15,31) DDR3_DRAMRST#
+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM
+0.75V_DDR_VTT
R149 *10K/J_4
+SMDDR_VREF
R162 0_6
R163 *10K/J_4
C325 470P/50V_4
R111 10K/F_4
R123 *M1@0_6
R116 10K/F_4
(7) VREF_DQ_DIMM0
R122 *M3@0_6
Place these Caps near So-Dimm0.
C252 10U/6.3V_6
C287 10U/6.3V_6
C271 10U/6.3V_6
C276 0.1U/16V_4
C308 0.1U/16V_4
C273 10U/6.3V_6
C262 10U/6.3V_6
C286 10U/6.3V_6
C265 0.1U/16V_4
C279 0.1U/16V_4
C278 0.1U/16V_4
C310 *330U/2V_7343
+SMDDR_VREF_DIMM
C326 0.1U/16V_4
C322 2.2U/6.3V_6
+SMDDR_VREF_DQ0
C206 0.1U/16V_4
C208 2.2U/6.3V_6
C365 2.2U/6.3V_6
C370 0.1U/16V_4
C389 1U/6.3V_4
C386 1U/6.3V_4
C378 1U/6.3V_4
C388 1U/6.3V_4
C373 10U/6.3V_6
C395 10U/6.3V_6
C374 10U/6.3V_6
Quanta Computer Inc.
PROJECT :ZR9
Size
Document Number
DDRIII SO-DIMM-0
Rev 1A
Date: Thursday, May 06, 2010
Sheet 14 of 47



Quanta Computer Inc.

PROJECT :ZR9

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

Date: Thursday, May 06, 2010 Sheet 15 of 47

N11P	AJ0N11P0T19
N11M	AJ0N11M0T20

SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only
CSP@ --> Operation P/N

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

U35A
fcbga973-nvidia-n11p-es-a1
COMMON

+1.05V_GFX

~ 500mA

C109 SW@0.1U/10V_4
C98 SW@0.1U/10V_4
C118 SW@1U/6.3V_4
C128 SW@1U/6.3V_4
C201 SW@4.7U/6.3V_6
C176 SW@4.7U/6.3V_6
C185 SW@10U/6.3V_8

AK16 AK17 AK21 AK24 AK27

PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5

+1.05V_GFX

1600mA

C127 SW@0.1U/10V_4
C97 SW@0.1U/10V_4
C96 SW@1U/6.3V_4
C138 SW@1U/6.3V_4
C171 SW@4.7U/6.3V_6
C167 SW@4.7U/6.3V_6
C202 SW@10U/6.3V_8

Near BGA

AG11 AG12 AG13 AG15 AG16 AG17 AG18 AG22 AG23 AG24 AG25 AG26 AJ14 AJ15 AJ19 AJ21 AJ22 AJ24 AJ25 AJ27 AK18 AK20 AK23 AK26 AL16

PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_IOVDDQ_15
PEX_IOVDDQ_16
PEX_IOVDDQ_17
PEX_IOVDDQ_18
PEX_IOVDDQ_19
PEX_IOVDDQ_20
PEX_IOVDDQ_21
PEX_IOVDDQ_22
PEX_IOVDDQ_23
PEX_IOVDDQ_24
PEX_IOVDDQ_25

+3V_GFX

C132 SW@4.7U/6.3V_6
C142 SW@1U/6.3V_4
C152 SW@0.1U/10V_4
C149 SW@0.1U/10V_4
C141 SW@0.1U/10V_4

J10 J11 J12 J13 J9

VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5

T6 T1 T8

AD20 D35 P7

VDD_SENSE
NC_9/ VDD_SENSE
NC_16/ VDD_SENSE

12~16 mils width 110mA

+1.05V_GFX

C161 SW@1U/6.3V_4
C108 SW@1U/6.3V_4

L3 SW@100nH_6

C133 SW@1U/6.3V_4
C144 SW@4.7U/6.3V_6

+PEX_PLLVDD

AD19 E35 R7 AG14

GND_SENSE
NC_10/ GND_SENSE
NC_17/ GND_SENSE

PEX_PLLVDD

12~16 mils width

+3V_GFX

L6 SW@0_6 +PEX_SVDD_3V3

AG19 F7

PEX_CAL_PD_VDDQ/ PEX_SVDD_3V3
NC_12/ PEX_SVDD_3V3

C117 SW@1U/6.3V_4

C162 SW@0.1U/10V_4
C164 SW@4.7U/6.3V_6

AG20 A2 AB7 AD6 AF6 AG6 AJ5 AK15 AL7 E7 H32 M7 P6 U7 V6

PEX_CAL_PU_GND/ NC
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_11
NC_13
NC_14
NC_15
NC_18
NC_19

PCI EXPRESS

PEX_RX0	AP17	PEG_TXP15	PEG_TXP15 (4)
PEX_RX0*	AN17	PEG_TXN15	PEG_TXN15 (4)
PEX_RX1	AN19	PEG_TXP14	PEG_TXP14 (4)
PEX_RX1*	AP19	PEG_TXN14	PEG_TXN14 (4)
PEX_RX2	AR19	PEG_TXP13	PEG_TXP13 (4)
PEX_RX2*	AR20	PEG_TXN13	PEG_TXN13 (4)
PEX_RX3	AP20	PEG_TXP12	PEG_TXP12 (4)
PEX_RX3*	AN20	PEG_TXN12	PEG_TXN12 (4)
PEX_RX4	AN22	PEG_TXP11	PEG_TXP11 (4)
PEX_RX4*	AP22	PEG_TXN11	PEG_TXN11 (4)
PEX_RX5	AR22	PEG_TXP10	PEG_TXP10 (4)
PEX_RX5*	AR23	PEG_TXN10	PEG_TXN10 (4)
PEX_RX6	AP23	PEG_TXP9	PEG_TXP9 (4)
PEX_RX6*	AN23	PEG_TXN9	PEG_TXN9 (4)
PEX_RX7	AN25	PEG_TXP8	PEG_TXP8 (4)
PEX_RX7*	AP25	PEG_TXN8	PEG_TXN8 (4)
PEX_RX8	AR25	PEG_TXP7	PEG_TXP7 (4)
PEX_RX8*	AR26	PEG_TXN7	PEG_TXN7 (4)
PEX_RX9	AP26	PEG_TXP6	PEG_TXP6 (4)
PEX_RX9*	AN26	PEG_TXN6	PEG_TXN6 (4)
PEX_RX10	AN28	PEG_TXP5	PEG_TXP5 (4)
PEX_RX10*	AP28	PEG_TXN5	PEG_TXN5 (4)
PEX_RX11	AR28	PEG_TXP4	PEG_TXP4 (4)
PEX_RX11*	AR29	PEG_TXN4	PEG_TXN4 (4)
PEX_RX12	AP29	PEG_TXP3	PEG_TXP3 (4)
PEX_RX12*	AN29	PEG_TXN3	PEG_TXN3 (4)
PEX_RX13	AN31	PEG_TXP2	PEG_TXP2 (4)
PEX_RX13*	AP31	PEG_TXN2	PEG_TXN2 (4)
PEX_RX14	AR31	PEG_TXP1	PEG_TXP1 (4)
PEX_RX14*	AR32	PEG_TXN1	PEG_TXN1 (4)
PEX_RX15	AR34	PEG_TXP0	PEG_TXP0 (4)
PEX_RX15*	AP34	PEG_TXN0	PEG_TXN0 (4)

PEX_TX0	AL17	PEG_RXP15_C	C130	SW@0.1U/10V_4	PEG_RXP15 (4)
PEX_TX0*	AM17	PEG_RXN15_C	C137	SW@0.1U/10V_4	PEG_RXN15 (4)
PEX_TX1	AM18	PEG_RXP14_C	C126	SW@0.1U/10V_4	PEG_RXP14 (4)
PEX_TX1*	AM19	PEG_RXN14_C	C120	SW@0.1U/10V_4	PEG_RXN14 (4)
PEX_TX2	AL19	PEG_RXP13_C	C119	SW@0.1U/10V_4	PEG_RXP13 (4)
PEX_TX2*	AK19	PEG_RXN13_C	C115	SW@0.1U/10V_4	PEG_RXN13 (4)
PEX_TX3	AL20	PEG_RXP12_C	C114	SW@0.1U/10V_4	PEG_RXP12 (4)
PEX_TX3*	AM20	PEG_RXN12_C	C110	SW@0.1U/10V_4	PEG_RXN12 (4)
PEX_TX4	AM21	PEG_RXP11_C	C107	SW@0.1U/10V_4	PEG_RXP11 (4)
PEX_TX4*	AM22	PEG_RXN11_C	C104	SW@0.1U/10V_4	PEG_RXN11 (4)
PEX_TX5	AL22	PEG_RXP10_C	C103	SW@0.1U/10V_4	PEG_RXP10 (4)
PEX_TX5*	AK22	PEG_RXN10_C	C95	SW@0.1U/10V_4	PEG_RXN10 (4)
PEX_TX6	AL23	PEG_RXP9_C	C88	SW@0.1U/10V_4	PEG_RXP9 (4)
PEX_TX6*	AM23	PEG_RXN9_C	C93	SW@0.1U/10V_4	PEG_RXN9 (4)
PEX_TX7	AM24	PEG_RXP8_C	C84	SW@0.1U/10V_4	PEG_RXP8 (4)
PEX_TX7*	AM25	PEG_RXN8_C	C86	SW@0.1U/10V_4	PEG_RXN8 (4)
PEX_TX8	AL25	PEG_RXP7_C	C81	SW@0.1U/10V_4	PEG_RXP7 (4)
PEX_TX8*	AK25	PEG_RXN7_C	C75	SW@0.1U/10V_4	PEG_RXN7 (4)
PEX_TX9	AL26	PEG_RXP6_C	C71	SW@0.1U/10V_4	PEG_RXP6 (4)
PEX_TX9*	AM26	PEG_RXN6_C	C65	SW@0.1U/10V_4	PEG_RXN6 (4)
PEX_TX10	AM27	PEG_RXP5_C	C63	SW@0.1U/10V_4	PEG_RXP5 (4)
PEX_TX10*	AM28	PEG_RXN5_C	C64	SW@0.1U/10V_4	PEG_RXN5 (4)
PEX_TX11	AL28	PEG_RXP4_C	C62	SW@0.1U/10V_4	PEG_RXP4 (4)
PEX_TX11*	AK28	PEG_RXN4_C	C61	SW@0.1U/10V_4	PEG_RXN4 (4)
PEX_TX12	AK29	PEG_RXP3_C	C58	SW@0.1U/10V_4	PEG_RXP3 (4)
PEX_TX12*	AL29	PEG_RXN3_C	C59	SW@0.1U/10V_4	PEG_RXN3 (4)
PEX_TX13	AM29	PEG_RXP2_C	C57	SW@0.1U/10V_4	PEG_RXP2 (4)
PEX_TX13*	AM30	PEG_RXN2_C	C54	SW@0.1U/10V_4	PEG_RXN2 (4)
PEX_TX14	AM31	PEG_RXP1_C	C48	SW@0.1U/10V_4	PEG_RXP1 (4)
PEX_TX14*	AM32	PEG_RXN1_C	C47	SW@0.1U/10V_4	PEG_RXN1 (4)
PEX_TX15	AN32	PEG_RXP0_C	C50	SW@0.1U/10V_4	PEG_RXP0 (4)
PEX_TX15*	AP32	PEG_RXN0_C	C52	SW@0.1U/10V_4	PEG_RXN0 (4)

PEX_REFCLK	AR16		CLK_PCIE_VGAP (10)
PEX_REFCLK*	AR17		CLK_PCIE_VGAN (10)
PEX_TSTCLK_OUT	AJ17	PEX_TSTCLK	R51 *SW@200/J_4
PEX_TSTCLK_OUT*	AJ18	PEX_TSTCLK#	
PEX_RST*	AM16	VGA_RST#	R456 *SW@0_4 PLTRST# (4,10,11,25,26,28,31,36)
PEX_CLKREQ*	AR13	PEX_CLKREQ#	R467 SW@10K/F_4 +3V_GFX
PEX_TERMP	AG21	PEX_TERMP	R49 SW@2.49K/F_4
TESTMODE	AP35	TESTMODE	R449 SW@10K/F_4
			R448 *SW@10K/F_4 +3V_GFX

R458 SW@100K_4

R457 SW@0_4 GPU_RST# (11)

R3589 un-mount for switchable function

Only for Hybrid

+3V_GFX

R80 SW@10K/F_4

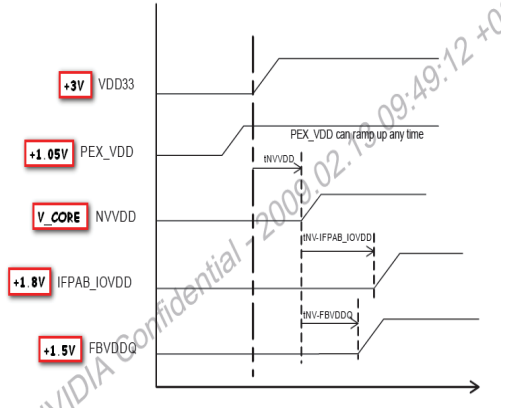
R489 SW@10K/F_4 +3V_S5

PEG_CLKREQ# (10)

Q20 SW@DTC144EUA

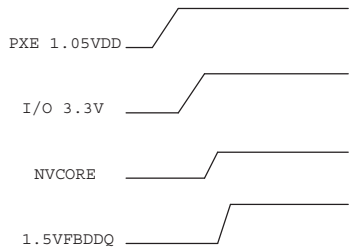
PEX_CLKREQ#

Q6 SW@DTC144EUA



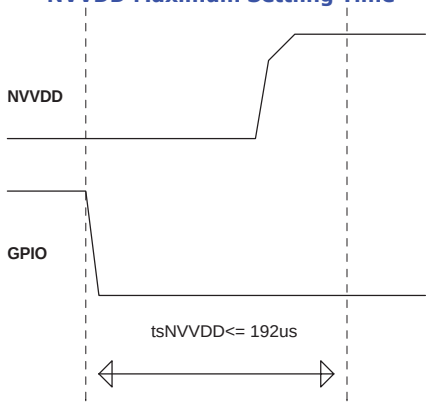
NVIDIA Confidential 12000.02.10 09:49:12 +0

power up sequence

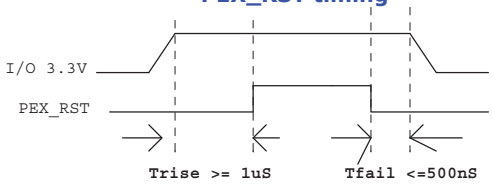


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing



Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE (PCIE I/F) 1/5	1A

Date: Thursday, May 06, 2010 Sheet 16 of 47

SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

N11P	AJ0N11P0T19
N11M	AJ0N11M0T20

U35B
fcbga973-nvidia-n11p-es-a1
COMMON

MEMORY I/F A

U35C
fcbga973-nvidia-n11p-es-a1
COMMON

MEMORY I/F C

Un-stuff for N11M
Stuff for N11P ,N11S

15mils width

For Debug only

15mils width

4/20 reserved for long run

All need stuff for N10P

N11P-GE1 Stuff 40.2 ohm
N11M-GE1 Stuff 60.4 ohm

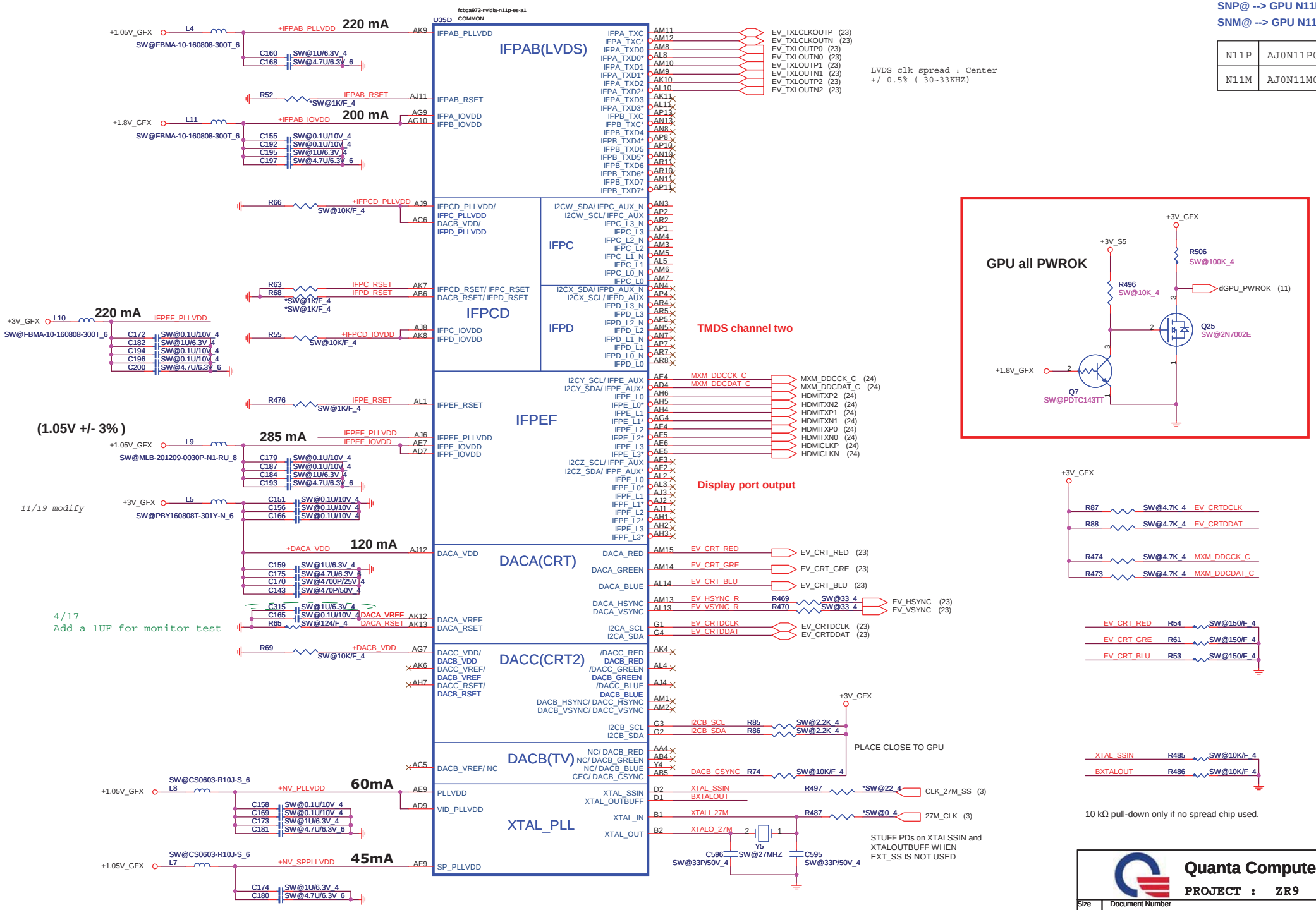
Quanta Computer Inc.
PROJECT : ZR9

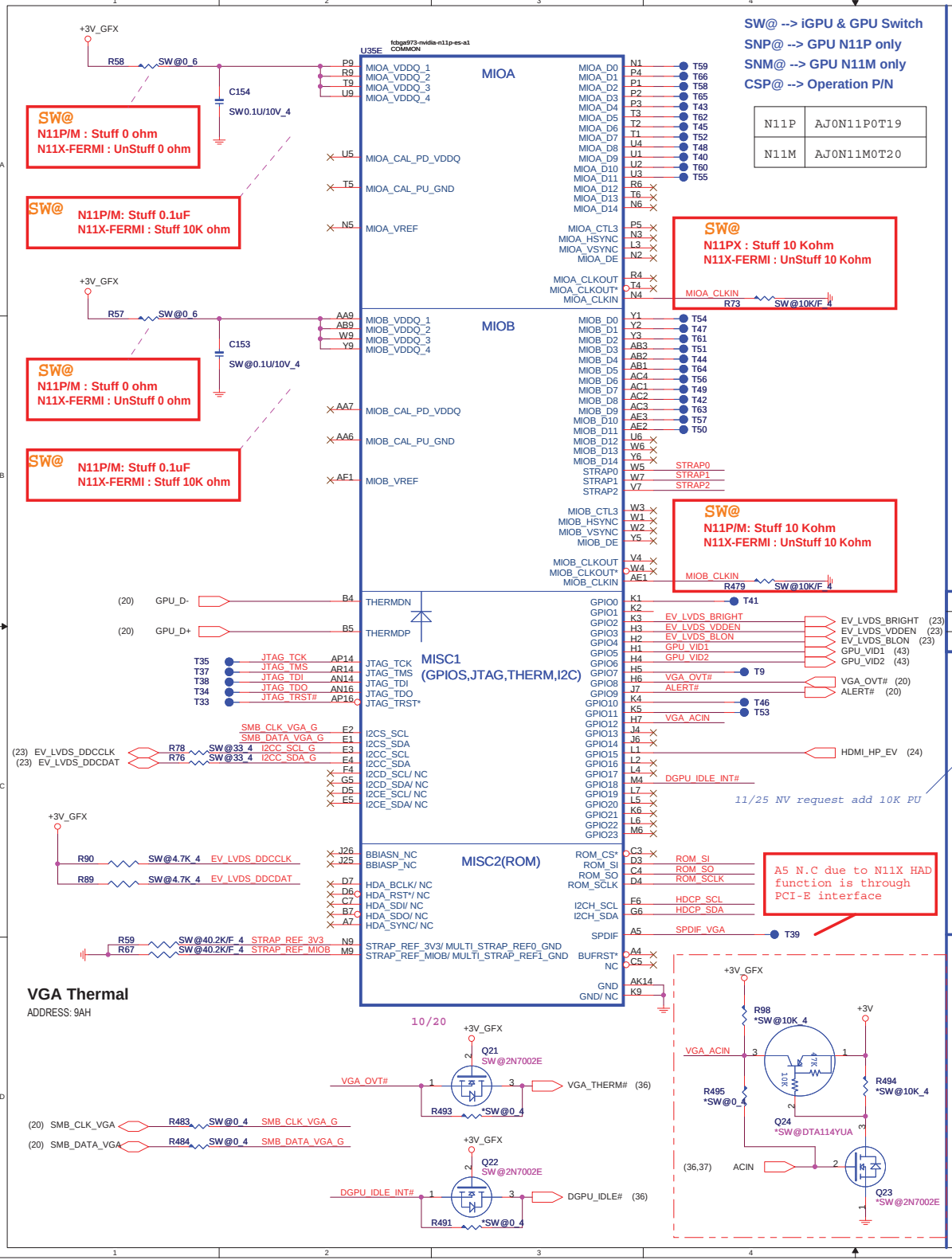
Size	Document Number	Rev
	N11P-GE (MEMORY I/F) 2/5	1A

Date: Thursday, May 06, 2010 Sheet 17 of 47

SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

N11P	AJ0N11P0T19
N11M	AJ0N11M0T20





SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only
CSP@ --> Operation P/N

N11P	AJ0N11P0T19
N11M	AJ0N11M0T20

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

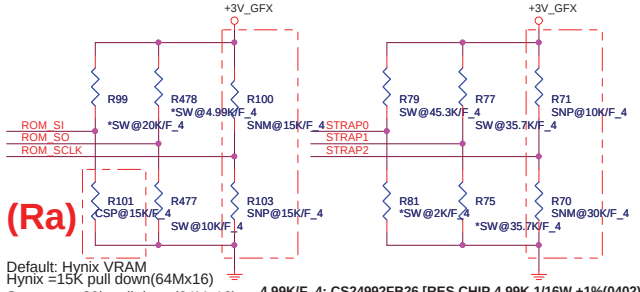
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)

AKD58GGT^01
AKD5LZGTW00
AKD5LGGT502

Logical Strap Bit Mapping

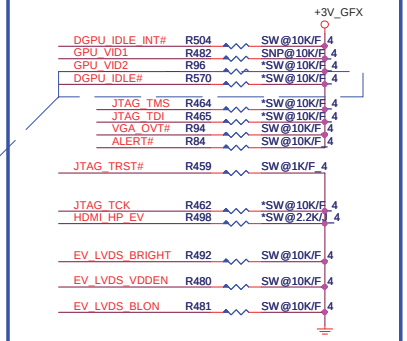
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM
Hynix =15K pull down(64Mx16)
Samsung =20k pull down(64Mx16)

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30K/F_4: CS33002JB23 [RES CHIP 30K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

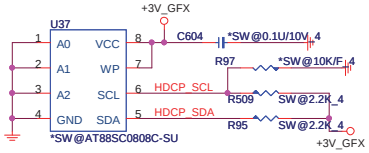
CHIP	ROM_SCLK	STRAP2	PCI_DEVID
N11M-GE1	PU 15K	PD 30K	0x0A75
N11P-GE1	PU 15K	PD 10K	0x0A29



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

HDCP ROM



Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

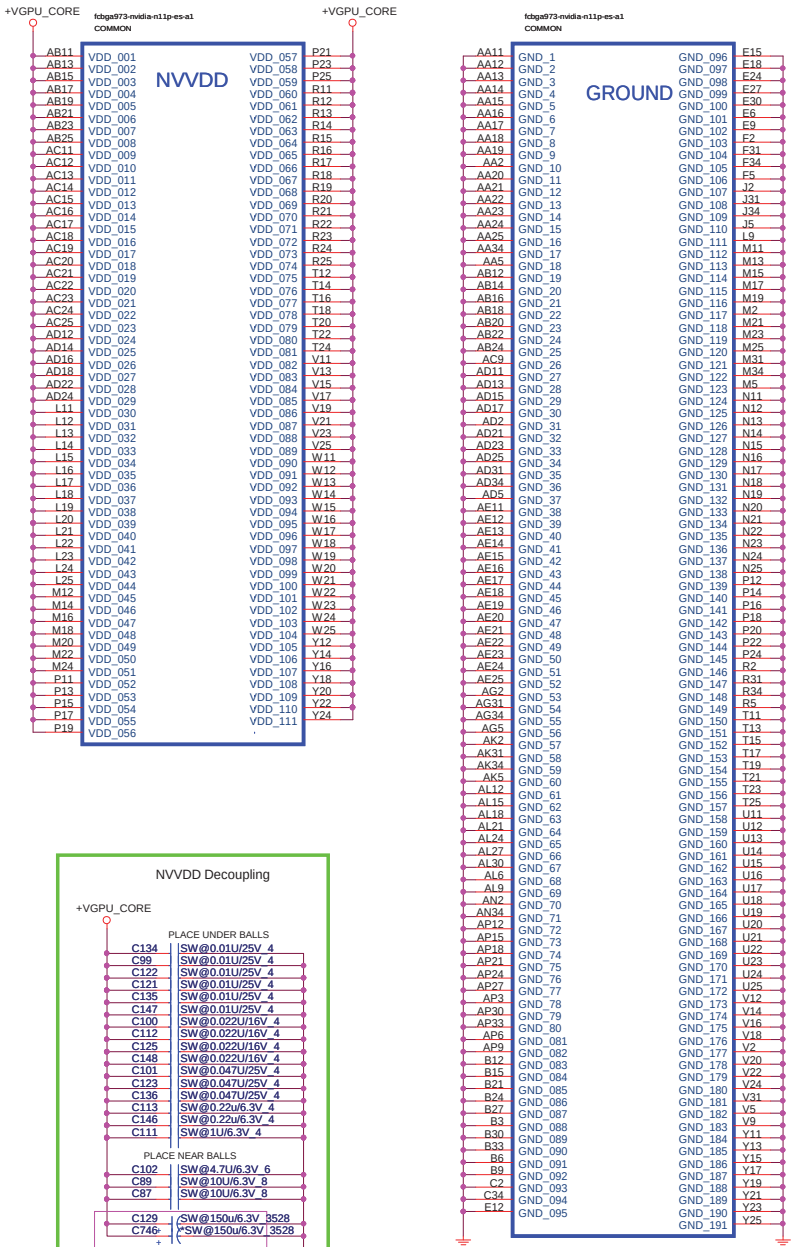
HDCP ROM reserve , Due to N11x had support internal HDCP function.

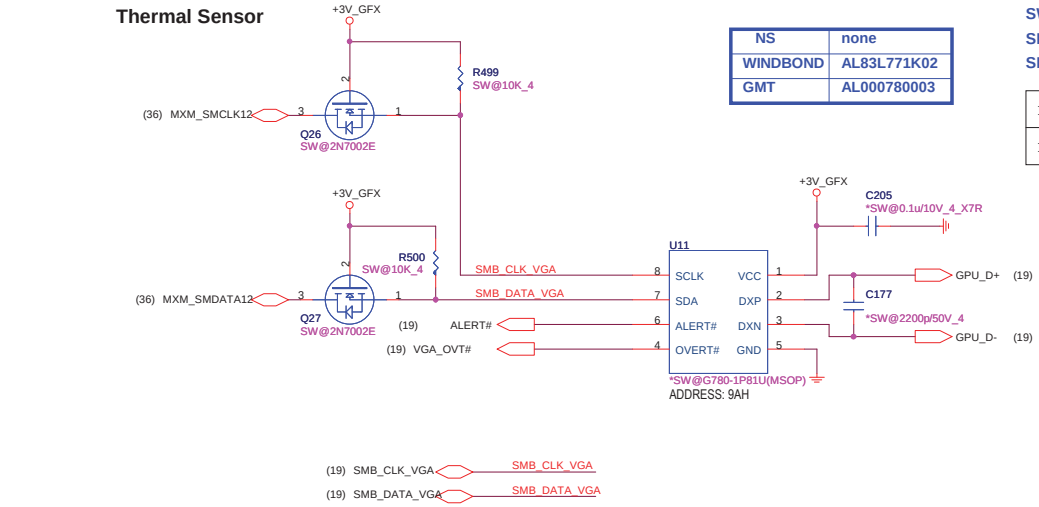
Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE (GPIO&STRAPS) 4/5	1A

Date: Thursday, May 06, 2010 Sheet 19 of 47

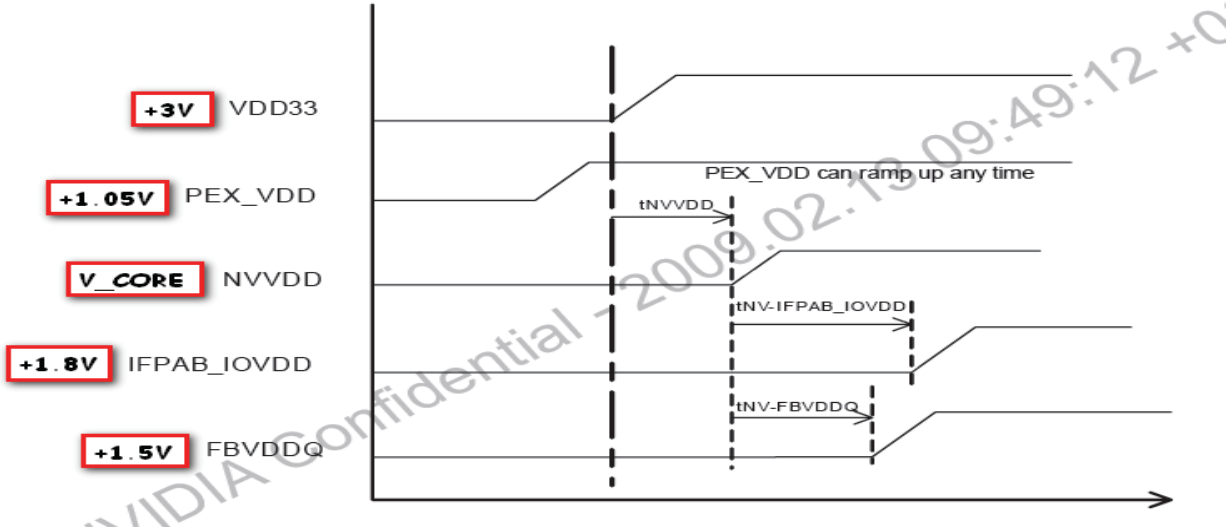




NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

N11P	AJ0N11P0T19
N11M	AJ0N11M0T20



NVIDIA Confidential - 2009.02.19 09:49:12 +0

Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE (POWER & GND&THM) 5/5	1A

Date: Thursday, May 06, 2010 Sheet 20 of 47

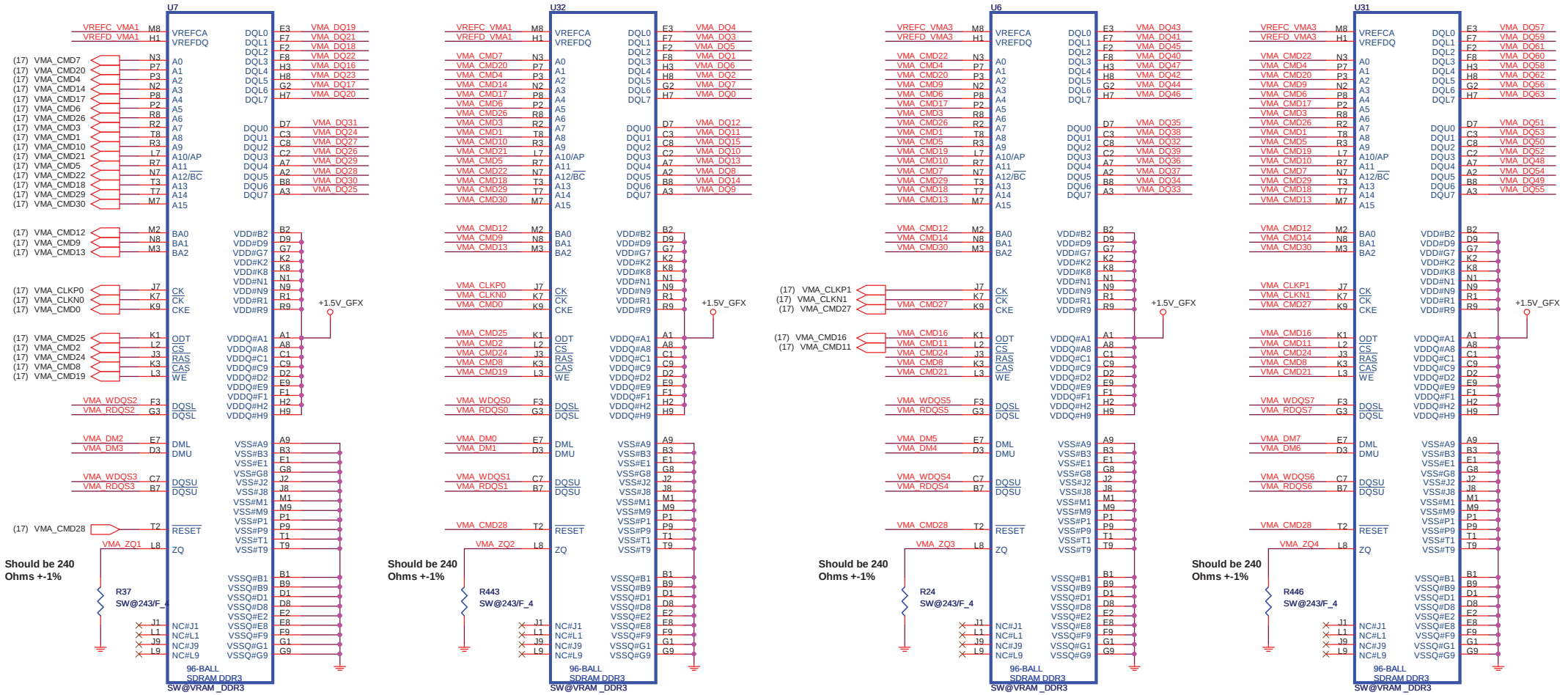
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

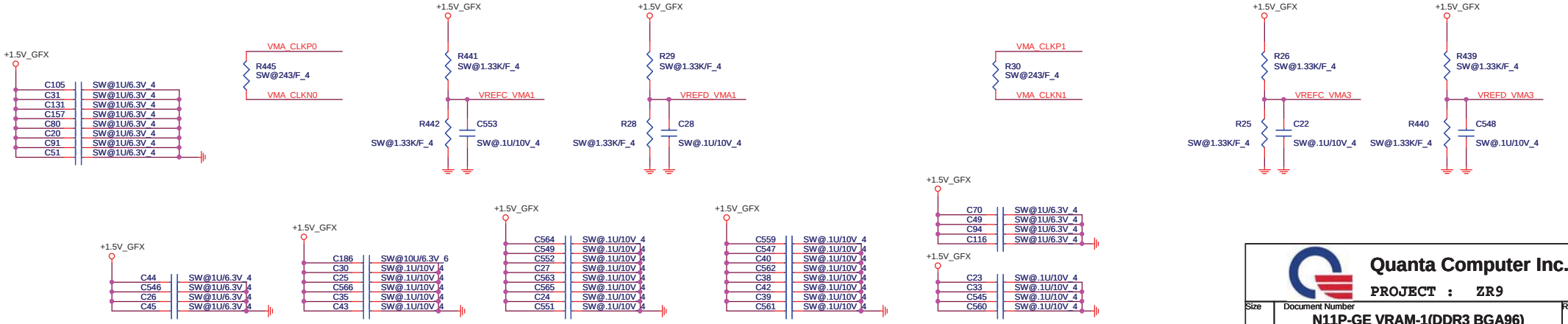
HYU	AKD5LZGTW04
SAM	AKD5LGGT506

(17) VMA_DQ[63..0]
(17) VMA_DM[7..0]
(17) VMA_WDQS[7..0]
(17) VMA_RDQS[7..0]

CHANNEL A: 256MB/512MB DDR3

(17,22,45) +1.5V_GFX





Quanta Computer Inc.

PROJECT : ZR9

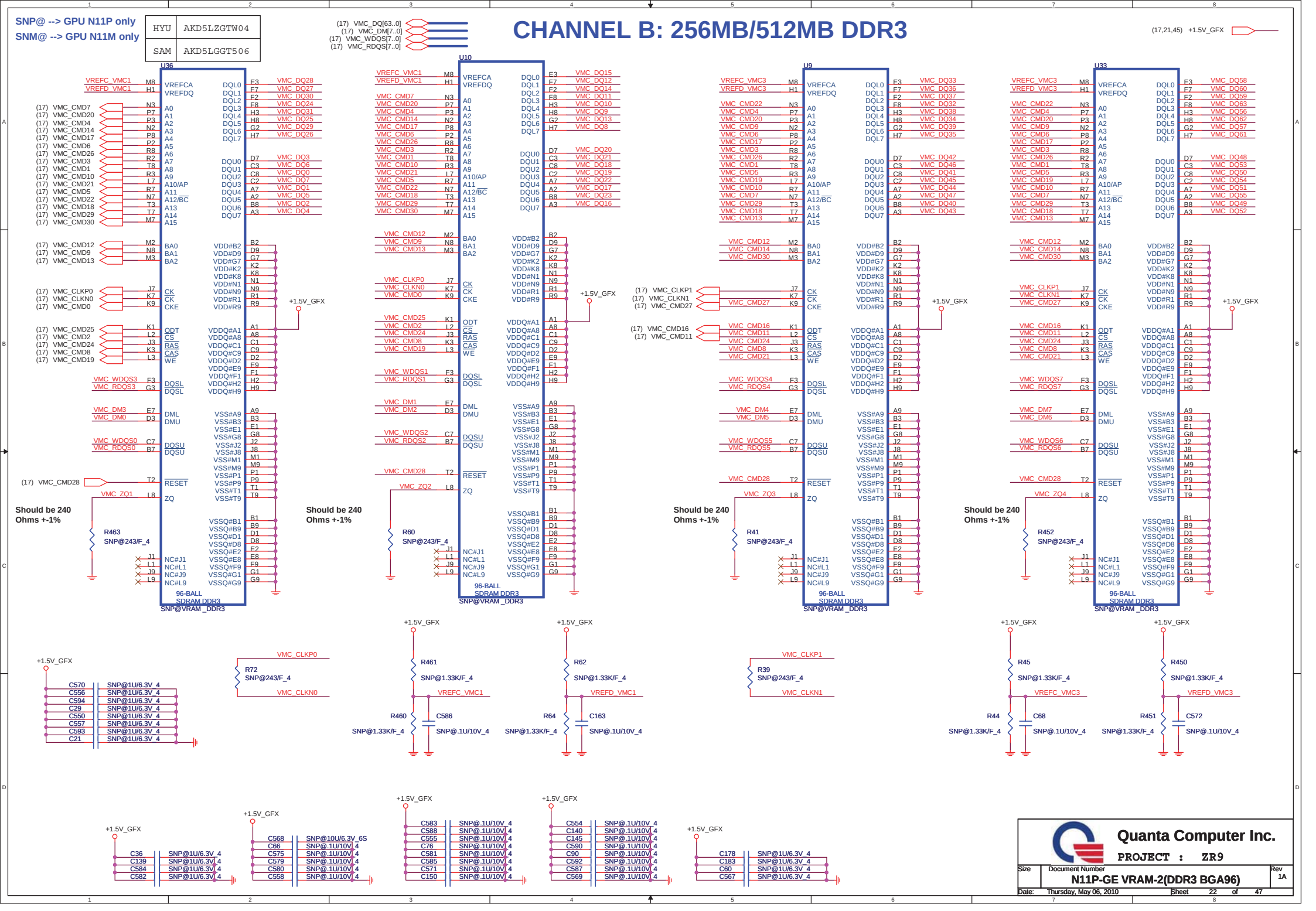
Size	Document Number	Rev
	N11P-GE VRAM-1(DDR3 BGA96)	1A

Date: Thursday, May 06, 2010 Sheet 21 of 47

SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

HYU	AKD5LZGTW04
SAM	AKD5LGGT506

CHANNEL B: 256MB/512MB DDR3



Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE VRAM-2(DDR3 BGA96)	1A

Date: Thursday, May 06, 2010 Sheet 22 of 47

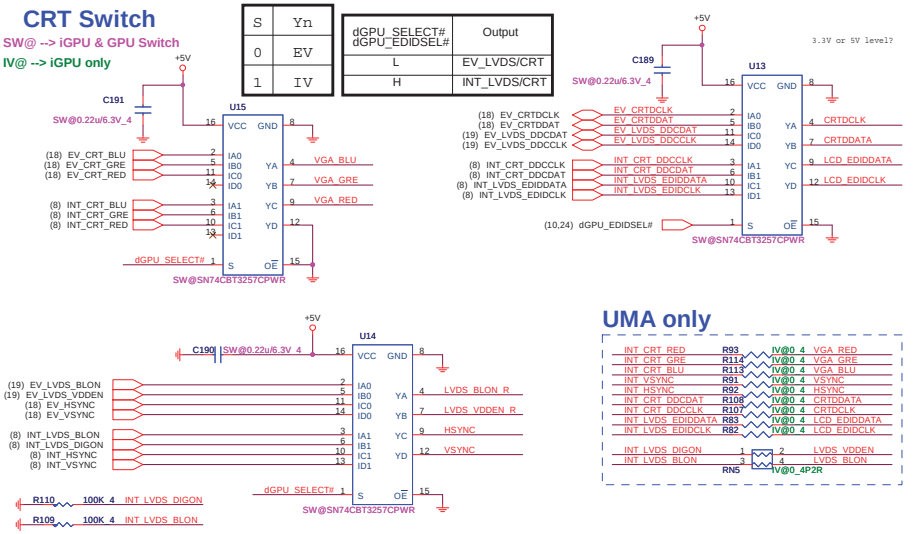
CRT Switch

SW@ --> iGPU & GPU Switch

IV@ --> iGPU only

S	Yn
0	EV
1	IV

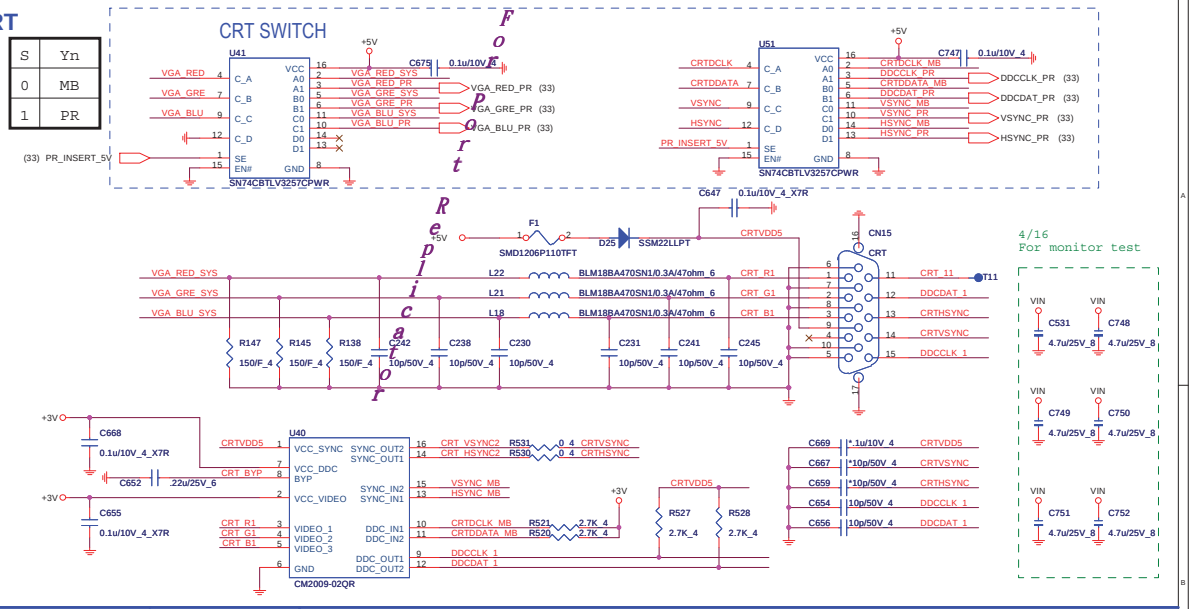
dGPU_SELECT# dGPU_EDIDSEL#	Output
L	EV_LVDS/CRT
H	INT_LVDS/CRT



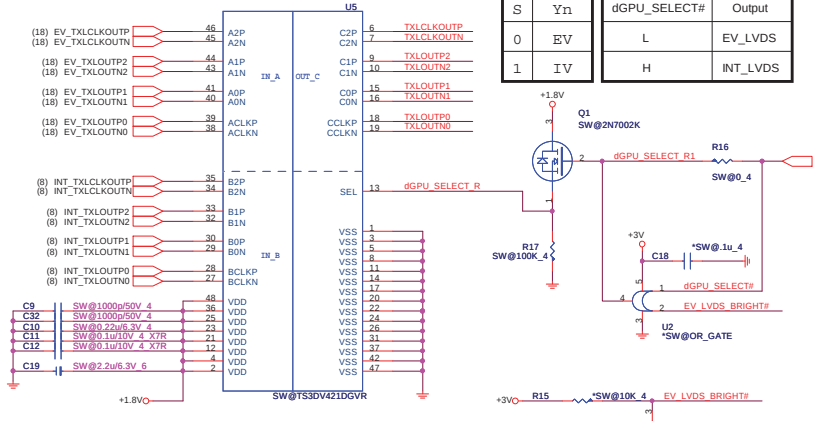
UMA only

CRT

S	Yn
0	MB
1	PR



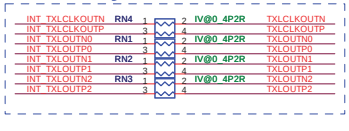
LVDS Switch



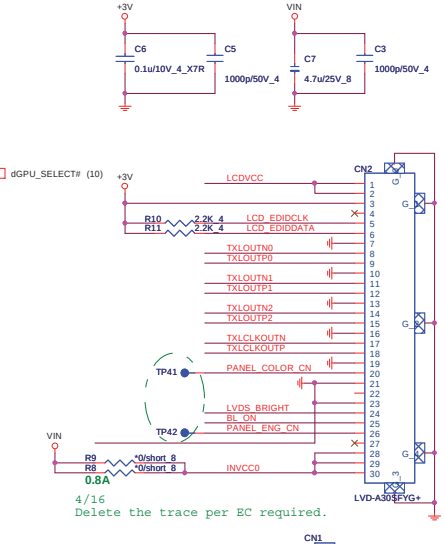
S	Yn
0	EV
1	IV

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

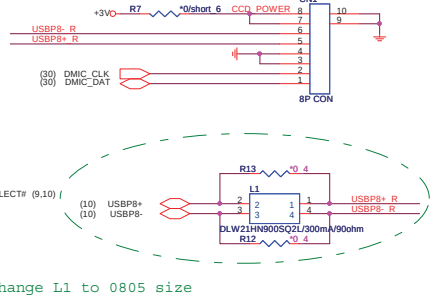
UMA only

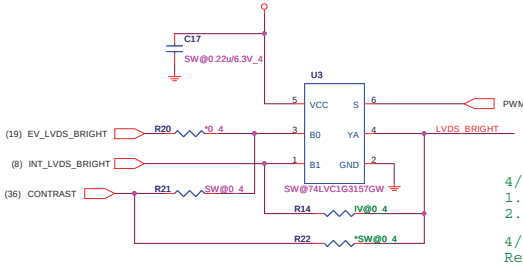


LVDS



4/16
Delete the trace per EC required.

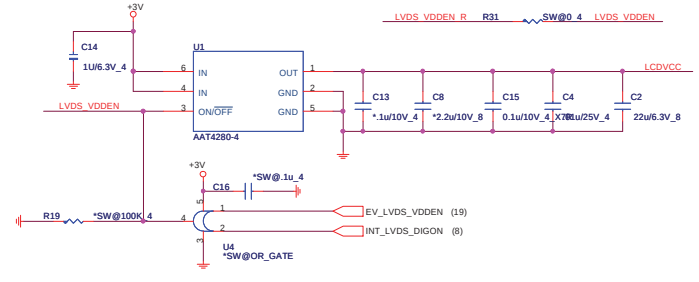




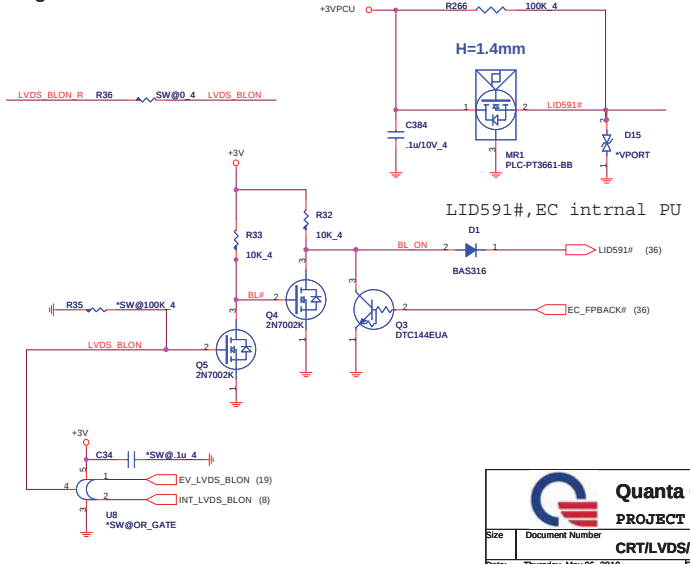
4/16
1. Change L1 to 0805 size
2. Change R12 , R13 from 0603 to 0402

4/20
Remove R12 , R13 and mount L1 for EMI requirement

LCD Power



Backlight Control



Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number	Rev
	CRT/LVDS/CCD/HALL	1A
Date: Thursday, May 06, 2010	Sheet 23 of 47	

I@ HDMI LEVEL SHIFTER

IV@ --> iGPU only
SW@ --> iGPU & GPU Switch
CSP@ --> Operation P/N

12/02 modify

Active Buffer

U22

from PCH

IV@DP139

Parade	AL008101000
TI	AL000139000

TI 3.9K	CS23902JB00
PS 499	CS14992FB24

from PCH

Control by pin4 HPDEN_R

Equalization Control

PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

close to pin2/11/15/21/26/33/40/46

NV HDMI-detect

To iGPU HPD

To NV HPD

OE# control for power saving

SDVO I2C Control

Quick Display

U18

SW@SN74CBT3257CPWR

S	Yn
0	EV
1	IV

UMA	CS22202JB18
SW	CS24702JB38

CSP@ HDMI SDVO I2C
For IV: 2.2K ohm
For SW:4.7K ohm

NV suggestion near HDMI connector

Switchable Graphic HDMI source

To Discrete

ESD Protect

close to HDMI connector

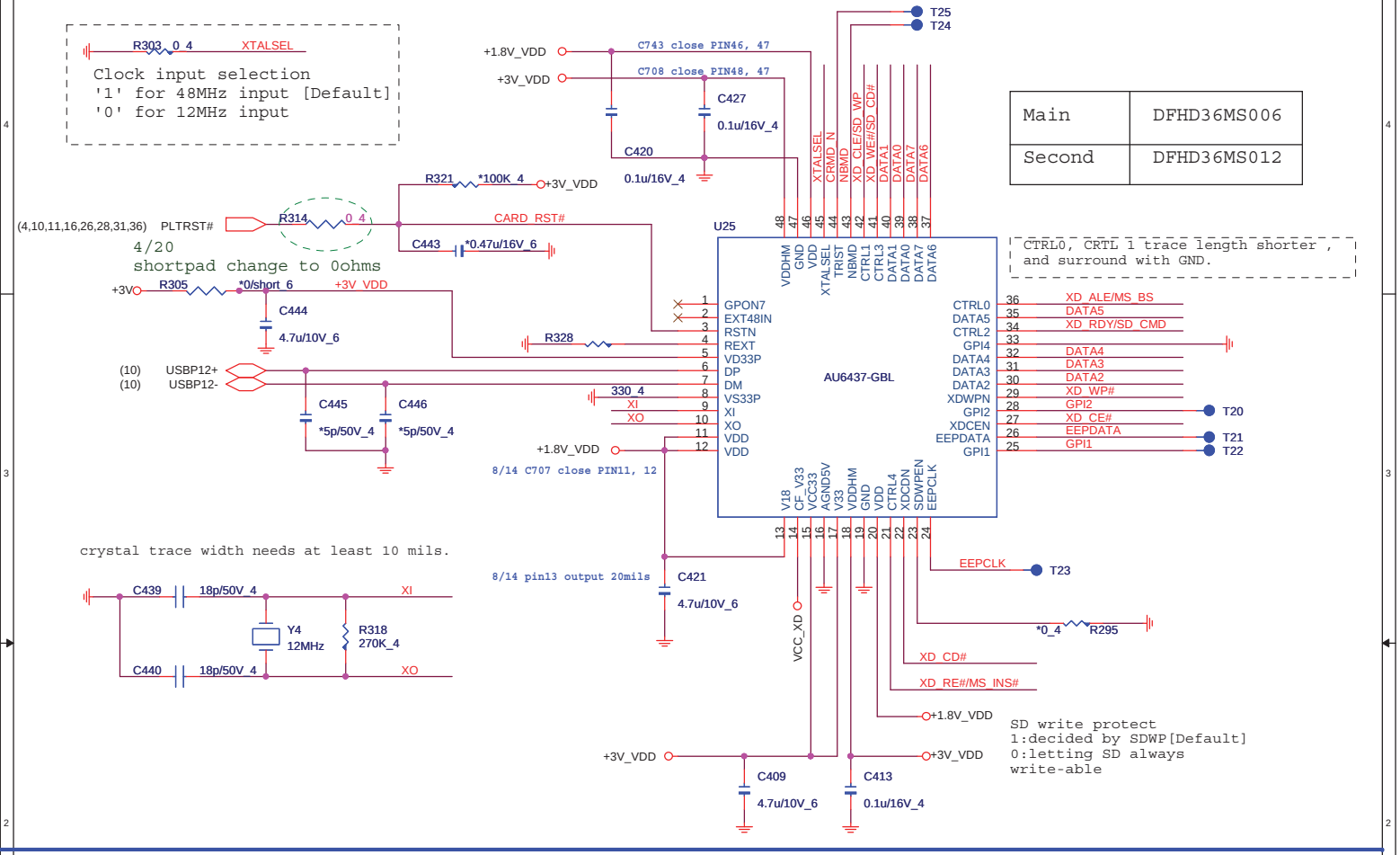
U44 U45 U19

*RClamp0524P

TO Port Replicat

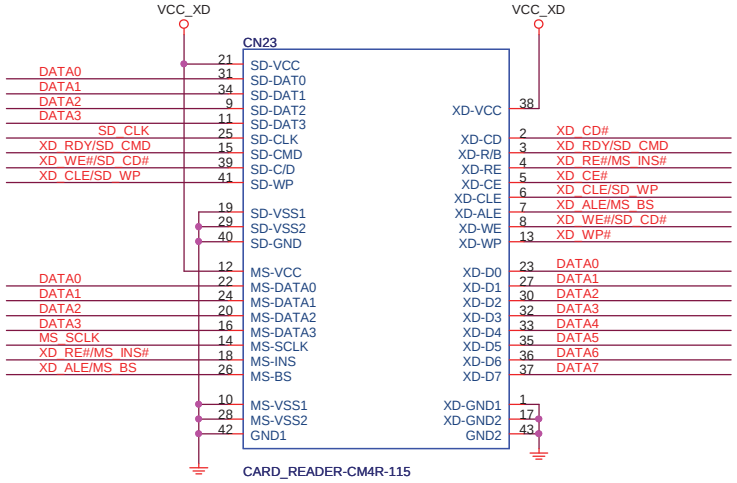
Quanta Computer Inc.
PROJECT : ZR9
DVI (PS8101)
Size | Document Number | Rev 1A
Date: Thursday, May 06, 2010 | Sheet 24 of 47

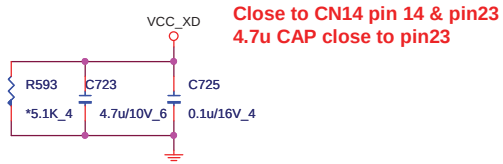
CARD READER Controller



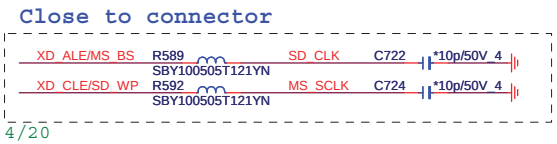
Main	DFHD36MS006
Second	DFHD36MS012

4 IN 1 CARD READER (MMC)





Close to CN14 pin 14 & pin23
4.7u CAP close to pin23



4/20
R589,R592 need to mount the bead SBY100505T121YN (CX05T121000) for EMI .

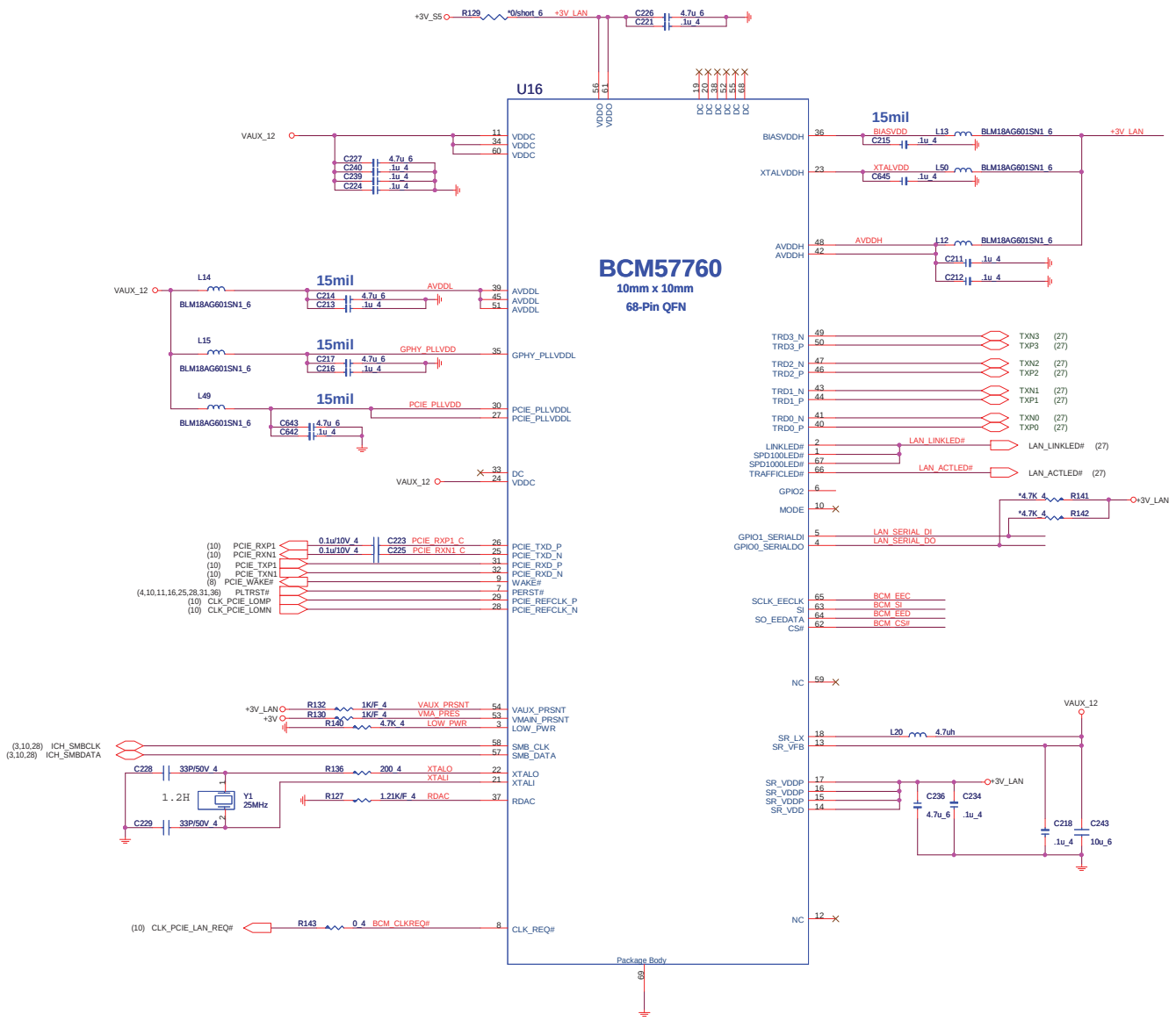
Quanta Computer Inc.

PROJECT : ZR9

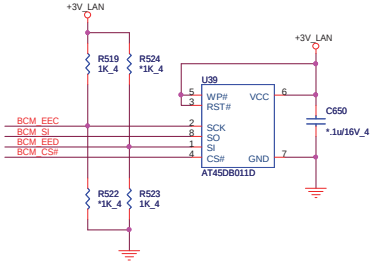
Size	Document Number	Rev
	AU6437 CardReader	1A

Date: Thursday, May 06, 2010 Sheet 25 of 47

Giga-LAN BCM57760(LAN)

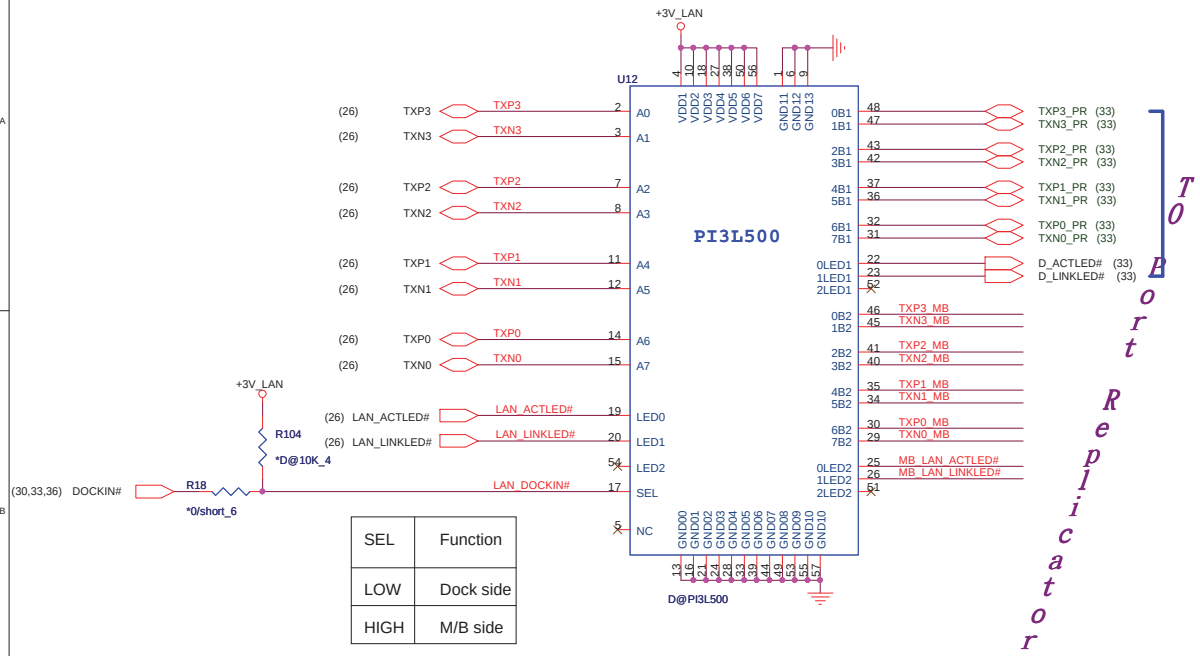


Flash (1M) for ASF2.0

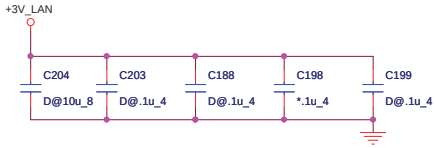


Quanta Computer Inc.			
PROJECT : ZR9			
Size	Document Number	LAN (BCM577760)	Rev 1A
Date: Thursday, May 06, 2010	Sheet 26 of 47		

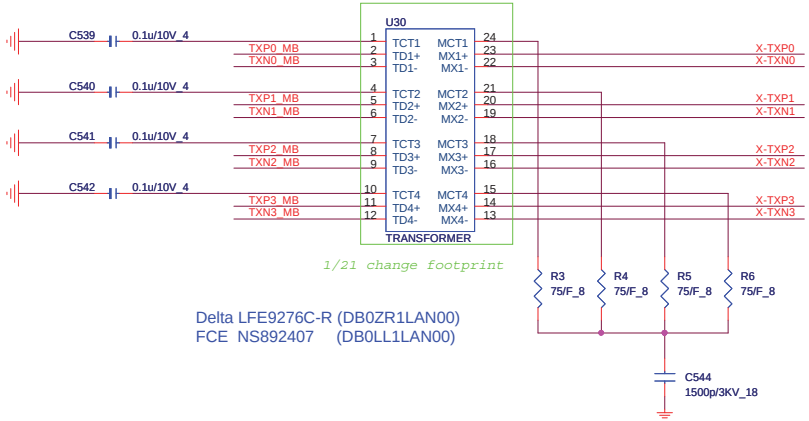
LAN SWITCH



SEL	Function
LOW	Dock side
HIGH	M/B side



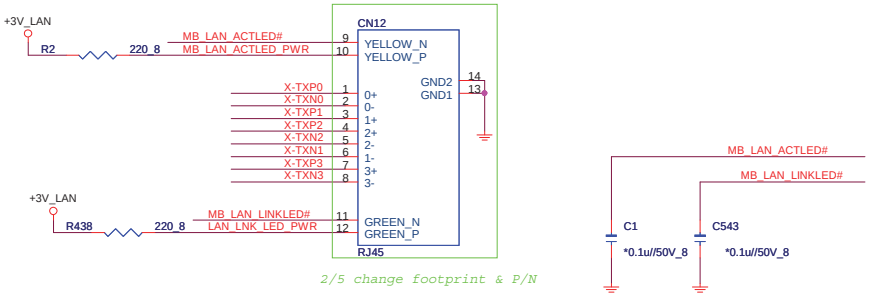
TRANSFORMER



1/21 change footprint

Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)

RJ45(LAN)



2/5 change footprint & P/N

Quanta Computer Inc.

PROJECT : ZR9

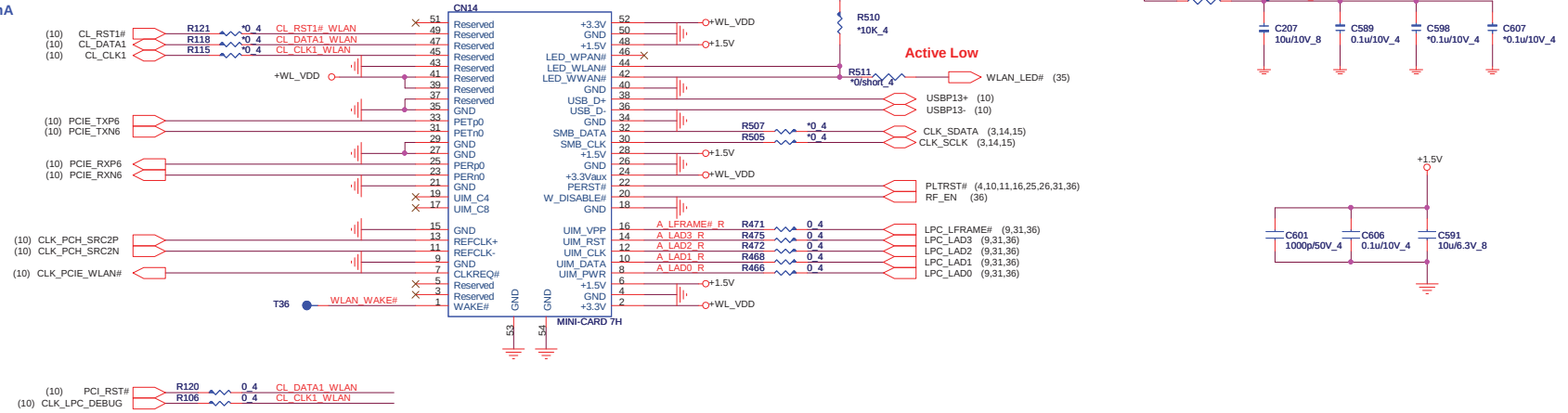
Size	Document Number	Rev
	LAN SWITCH/TRANSFORMER/RJ45	1A

Date: Thursday, May 06, 2010 Sheet 27 of 47

MINI-CARD WLAN(MPC)

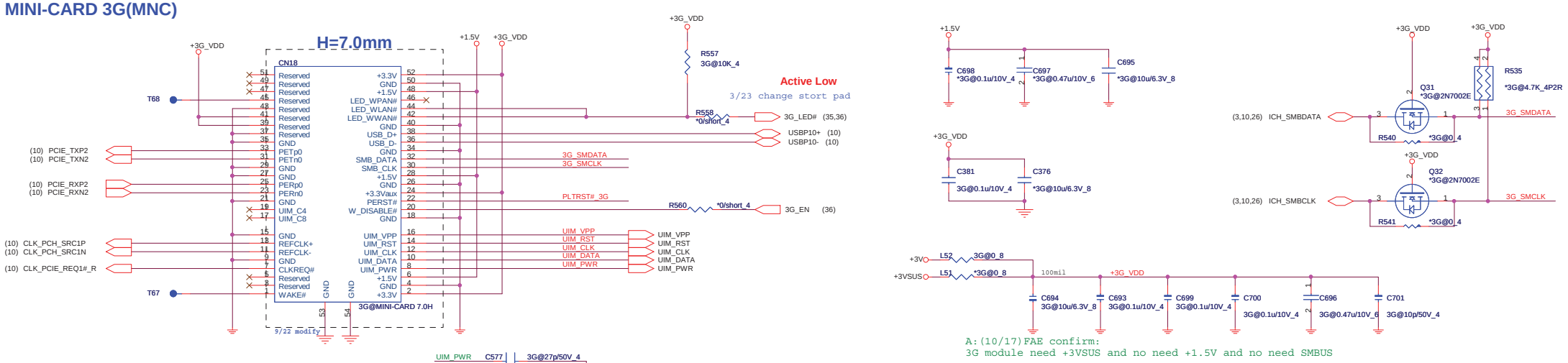
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

H=5.6mm



MINI-CARD 3G(MNC)

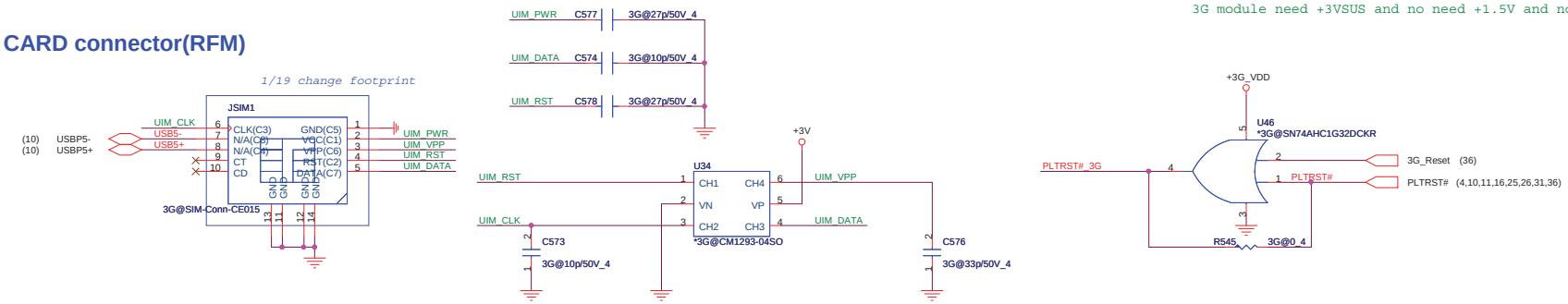
H=7.0mm



A:(10/17)FAE confirm:
3G module need +3VSUS and no need +1.5V and no need SMBUS

SIM CARD connector(RFM)

1/19 change footprint



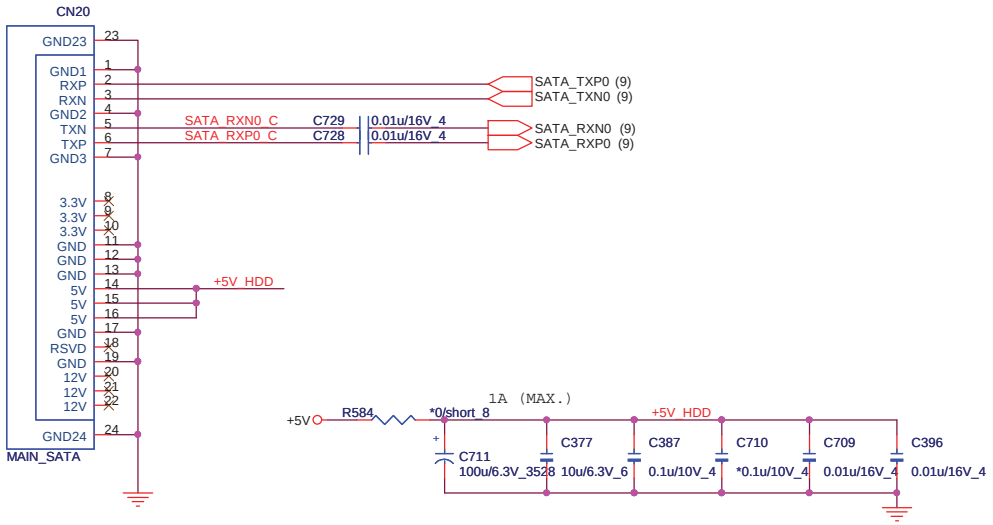
Quanta Computer Inc.

PROJECT : ZR9

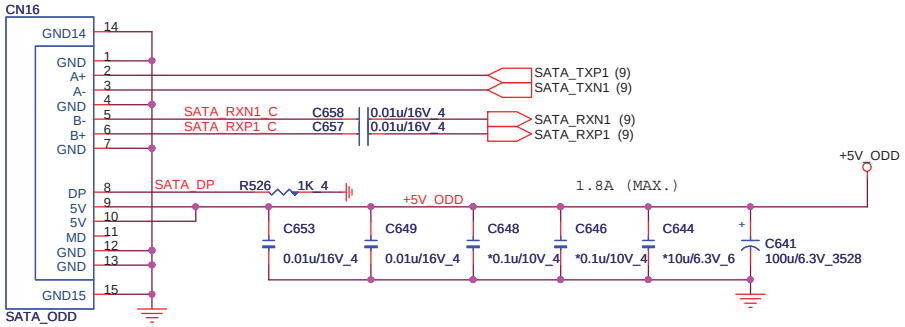
Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A

Date: Thursday, May 06, 2010 Sheet 28 of 47

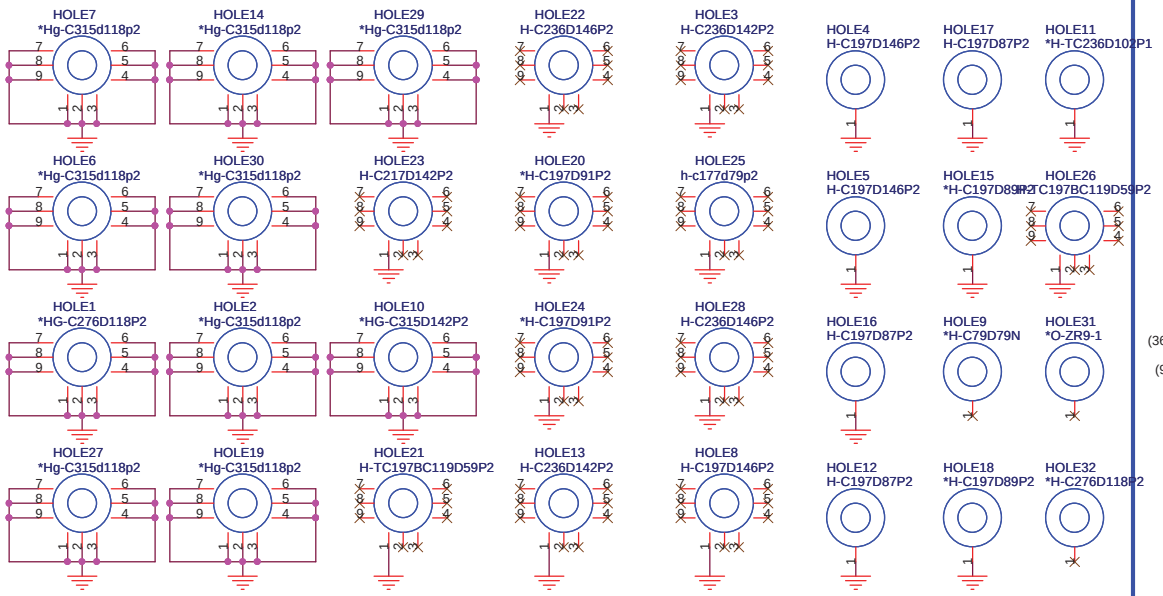
SATA HDD(HDD)



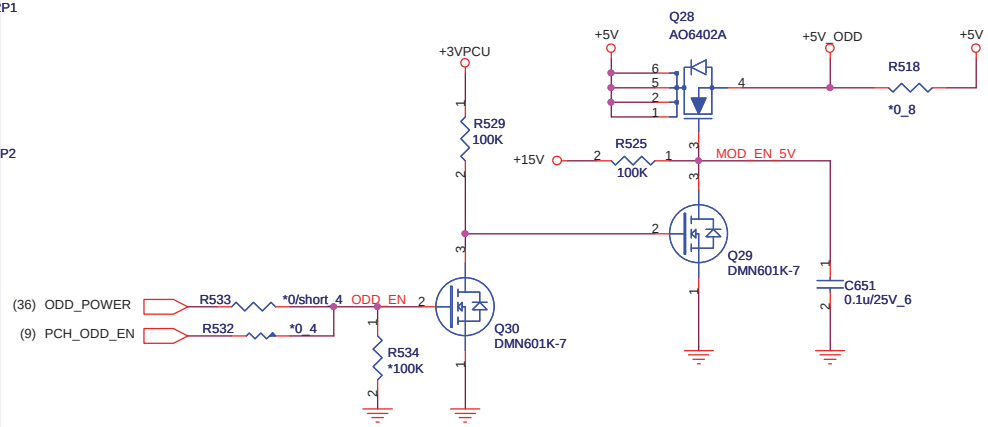
SATA ODD (ODD)



HOLE(OTH)



ODD POWER(ODD)



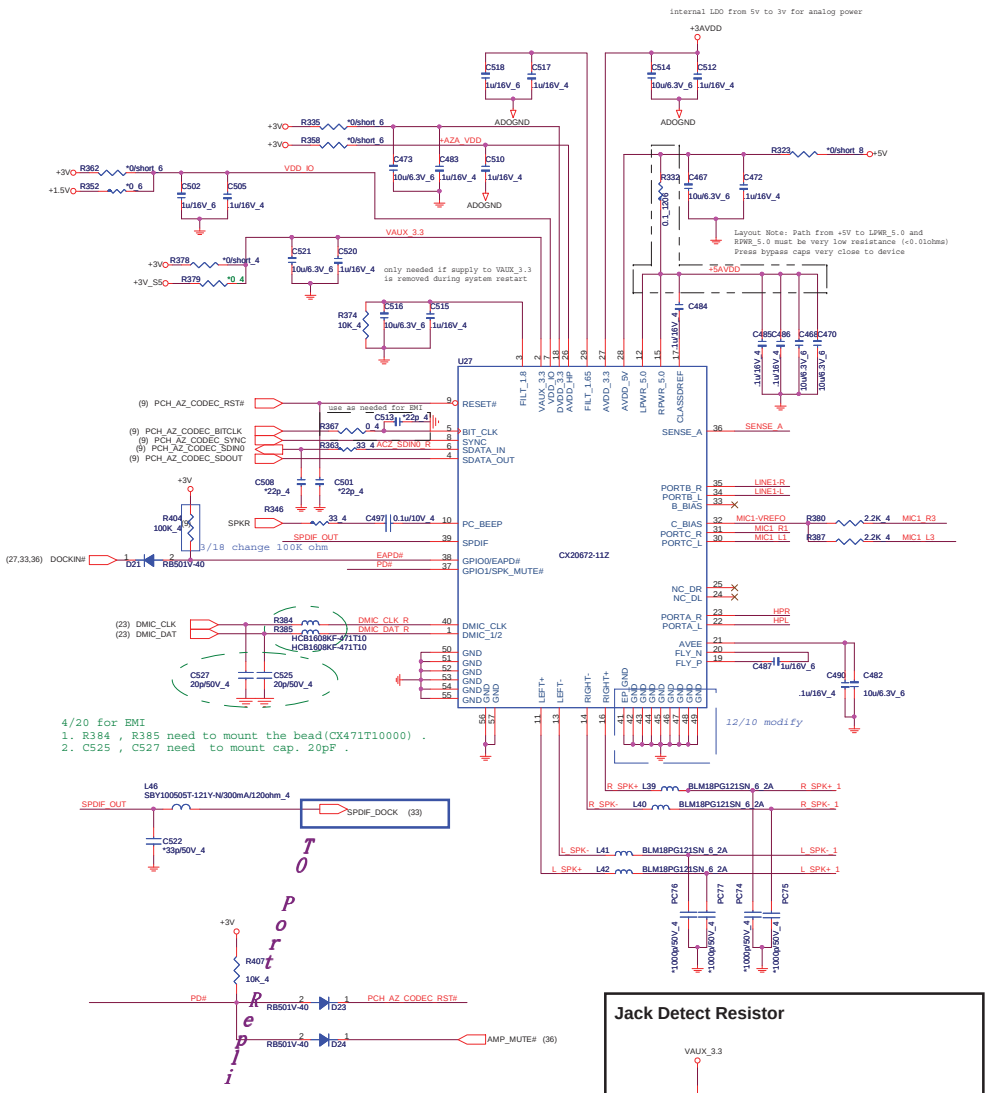
Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A

Date: Thursday, May 06, 2010 Sheet 29 of 47



EXTERNAL MIC

conn and 線路follow ZQ1 and Z06, 但C and R值follow conexant

3/19 change to X7R type

Max. 100mVrms input for Mic-IN

11/27 change to ADOGND

Normal OPEN Jack

11/17 modify

Near CN28

LINE-OUT/SPDIFO(AMP)

conn and 線路follow ZQ1, 但C值follow conexant

11/27 change to ADOGND

Normal OPEN Jack

11/17 modify

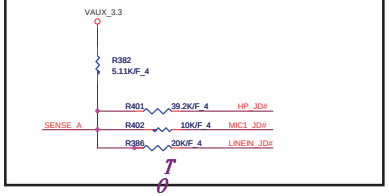
Near CN25

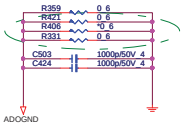
INT SPEAKER CONN

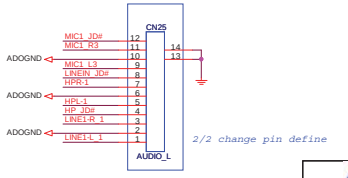
40mil for each signal

conn and 線路follow ZR7, 但C值follow conexant

Jack Detect Resistor







4/20 EMI suggested that R421 , R331 need to be mounted .

Quanta Computer Inc.

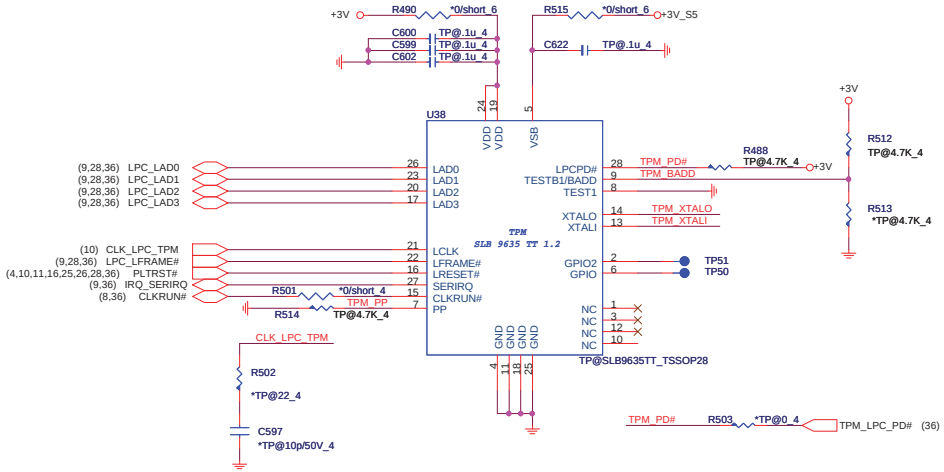
PROJECT : ZR9

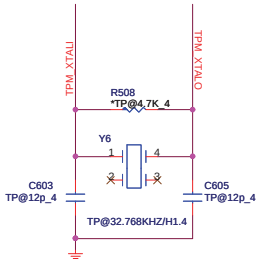
Size	Document Number	Rev
	CX20672-11Z/MIC/HP/SPK	1A

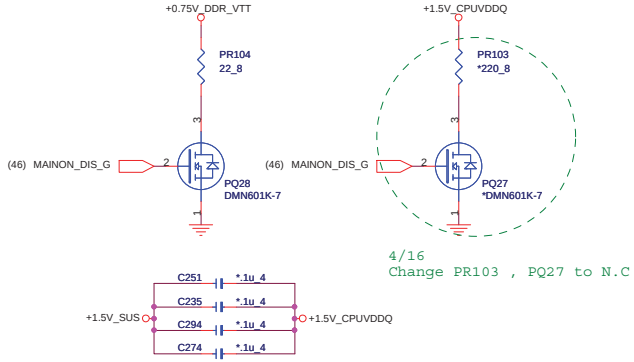
Date: Thursday, May 06, 2010 Sheet 30 of 47

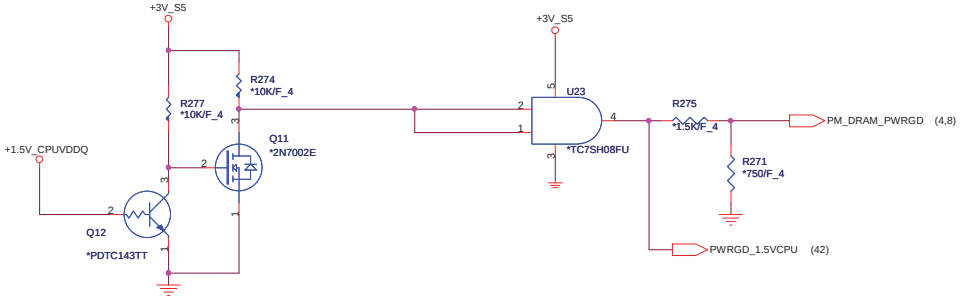
Trust Platform Module(Reserved)

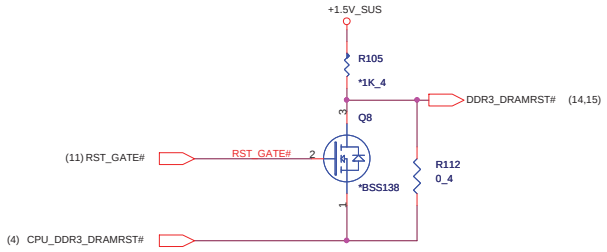
	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

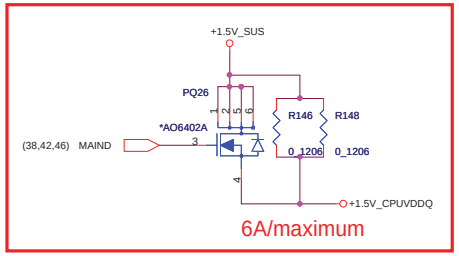












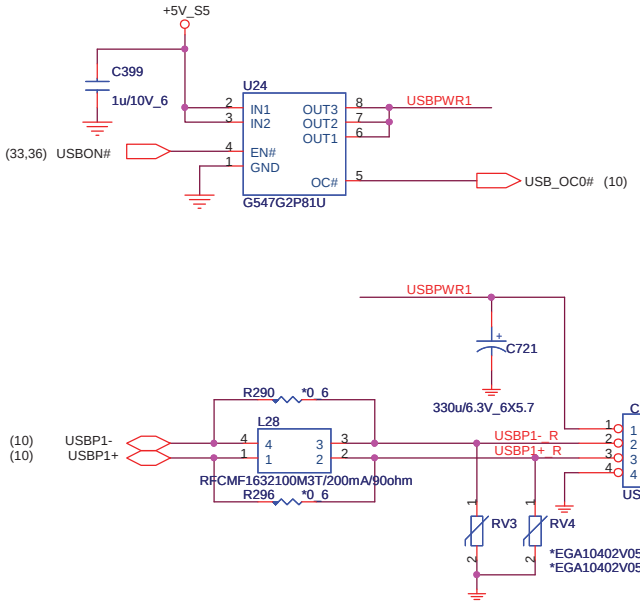
Quanta Computer Inc.

PROJECT : ZR9

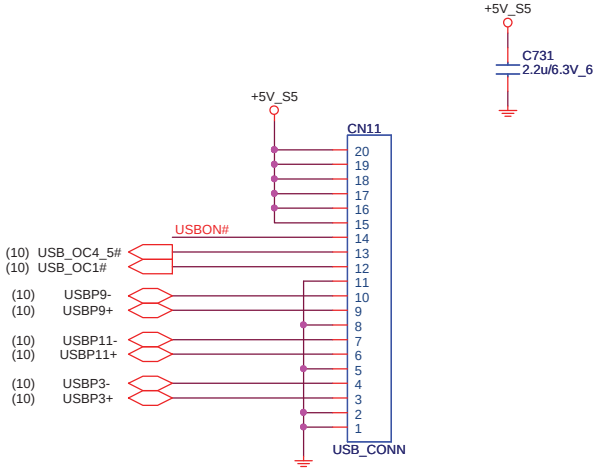
Size	Document Number	Rev
	TPM/ S3 POWER SAVING	1A

Date: Thursday, May 06, 2010 Sheet 31 of 47

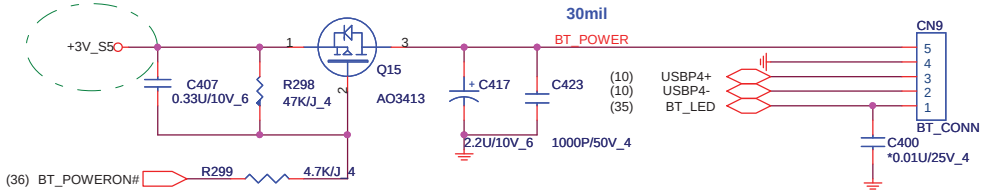
USB PORT(USB)



USB BOARD CONN(USB)



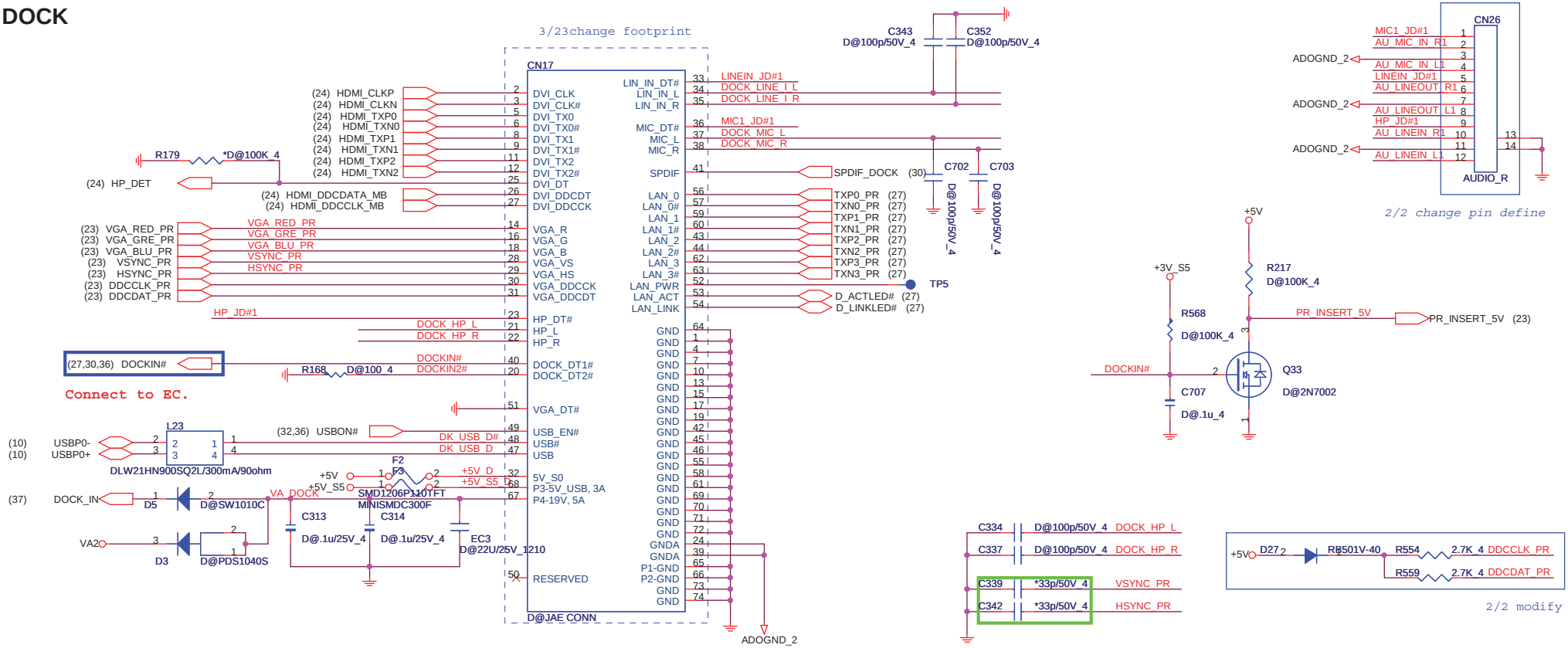
BLUETOOTH CONNECTOR



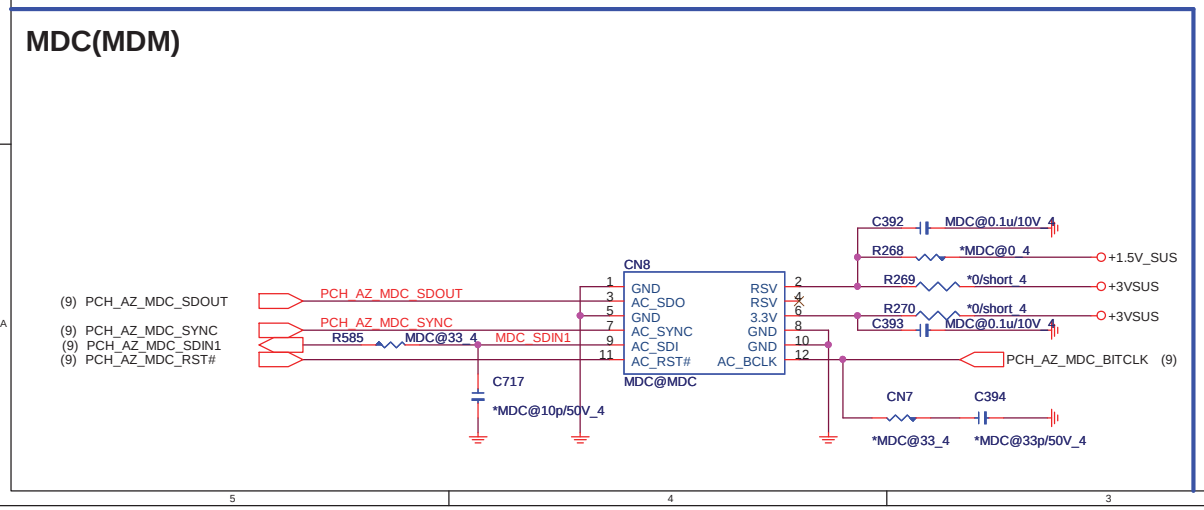
4/16 modify power from +3V to +3V_S5

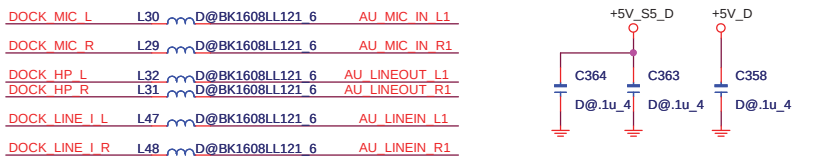
Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: BT/USB/USB DB	Rev 1A
Date: Wednesday, May 05, 2010	Sheet 32 of 47	

CABLE DOCK



MDC(MDM)



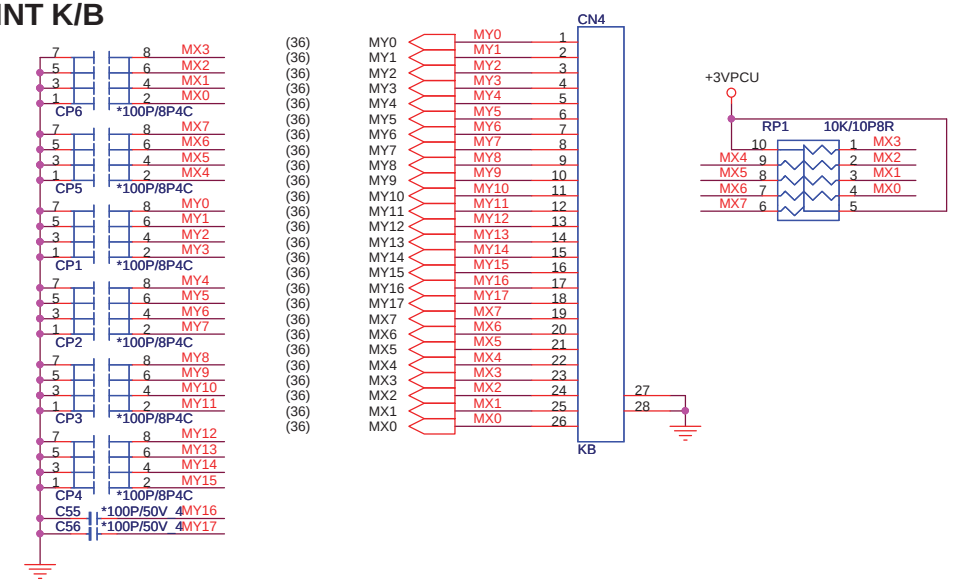


Quanta Computer Inc.

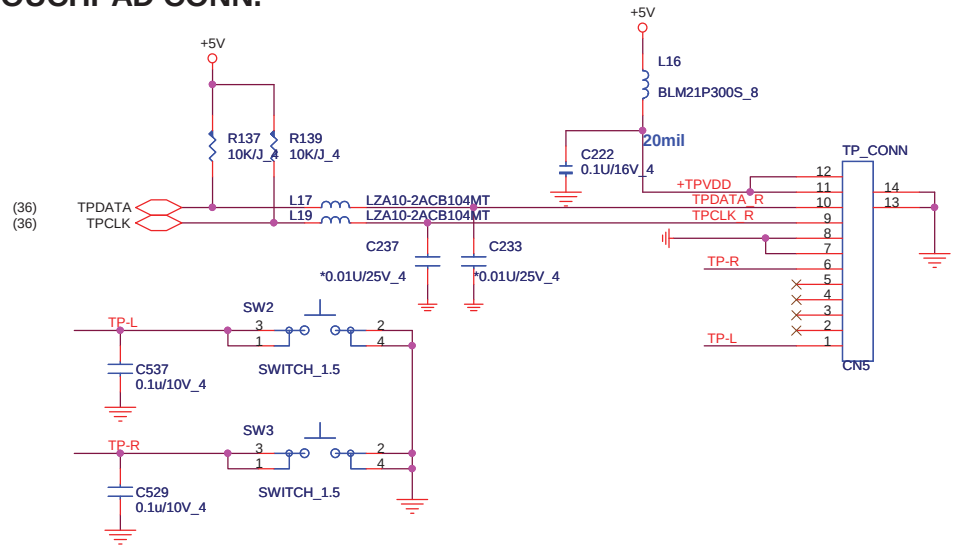
PROJECT : ZR9

Size	Document Number	Rev
	Docking / MDC	1A
Date: Thursday, May 06, 2010	Sheet 33 of 47	

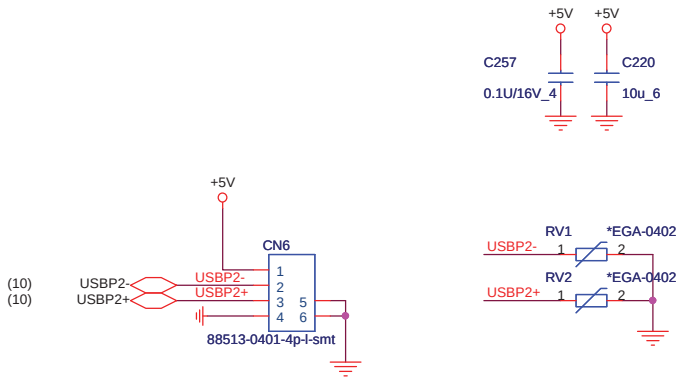
INT K/B



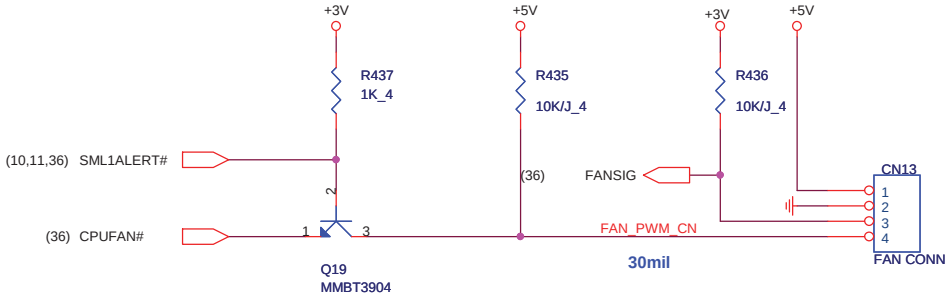
TOUCHPAD CONN.



Finger-Printer CONN.



CPU FAN



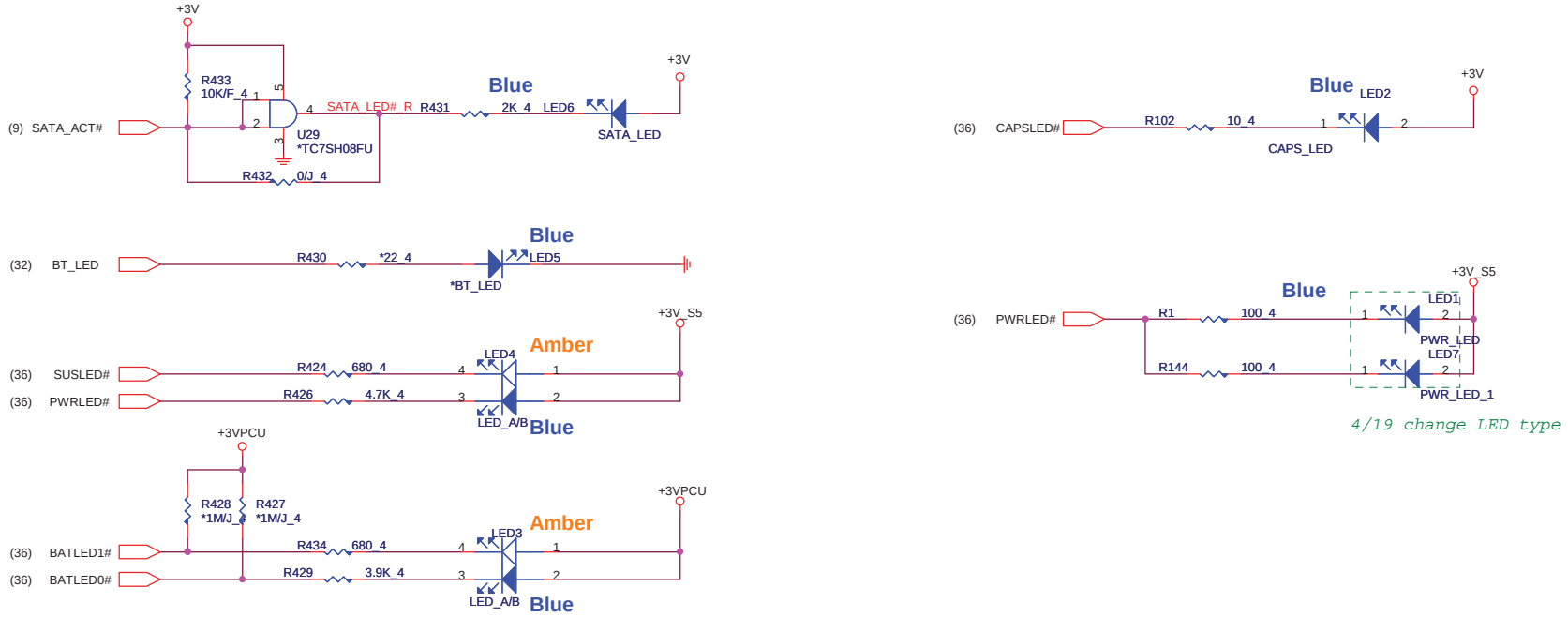
Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	KB/TP+FP/FAN	1A

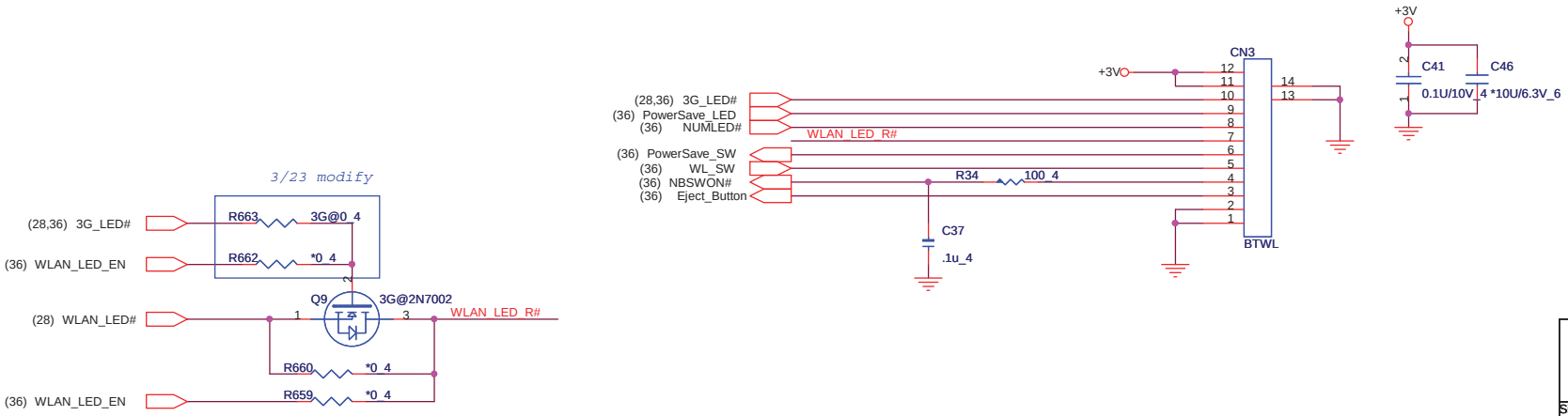
Date: Thursday, May 06, 2010 Sheet 34 of 47

M/B LED



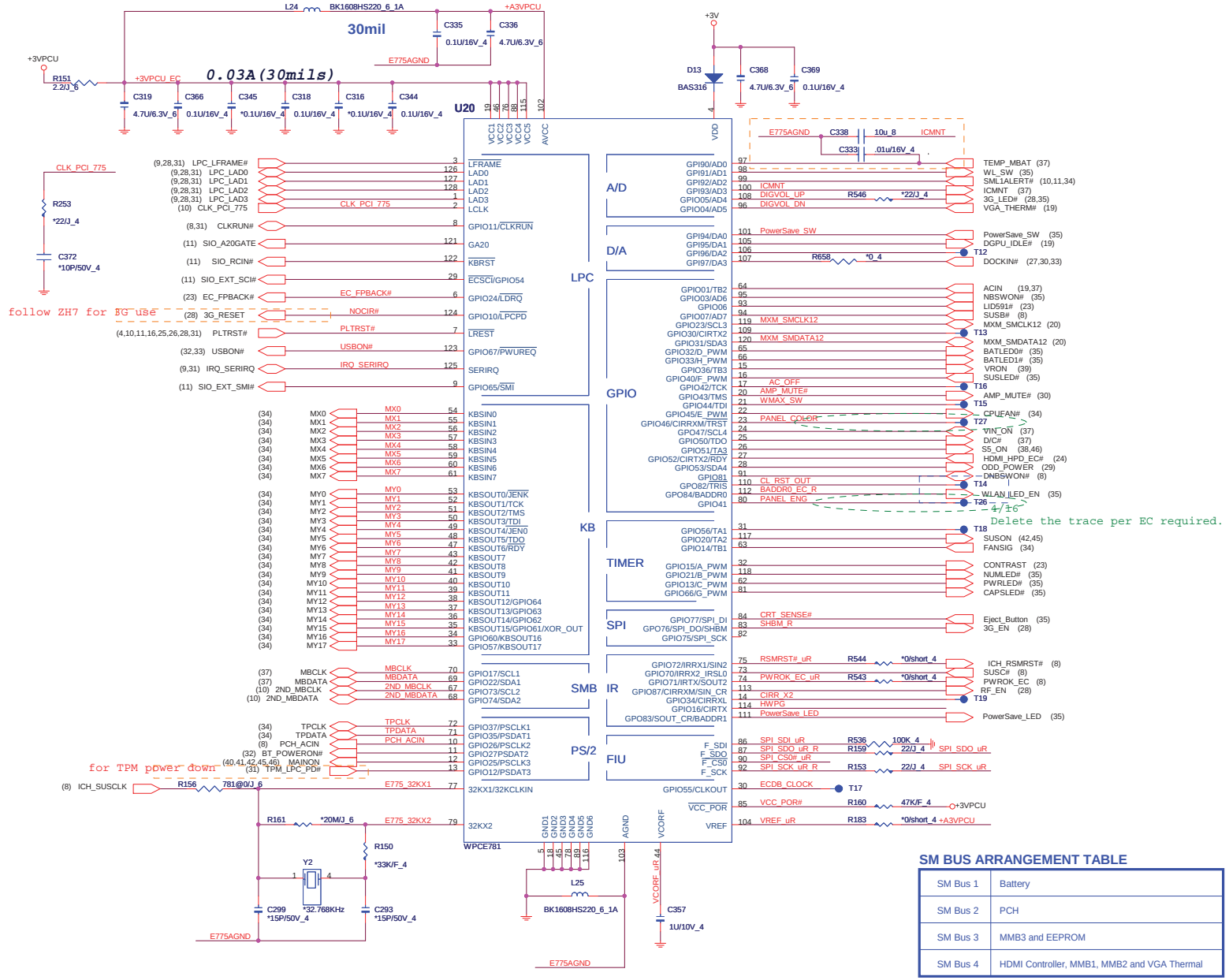
4/19 change LED type

POWER D/B CONNECTOR



Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: POWER/DB/LED	Rev 1A
Date: Thursday, May 06, 2010	Sheet 35 of 47	

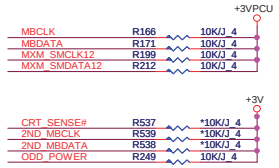
EC



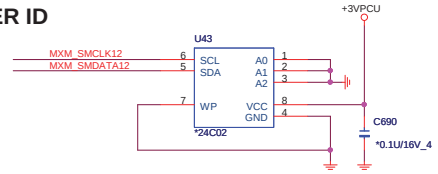
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

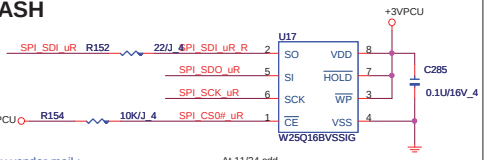
SM BUS PU



ACER ID



SPI FLASH

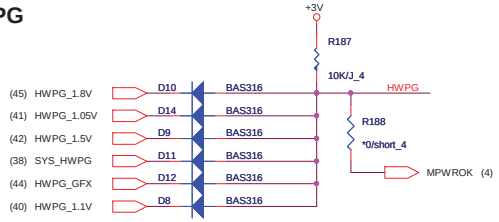


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

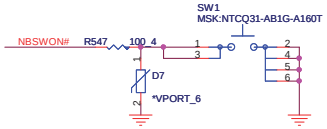
At 11/24 add

Winbond	W25X16AVSSIG	AKE38ZP0N01
MXIC	MX25L1605AM2C-15G	AKE37FP0Z13
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

HWPG



POWER-ON Switch



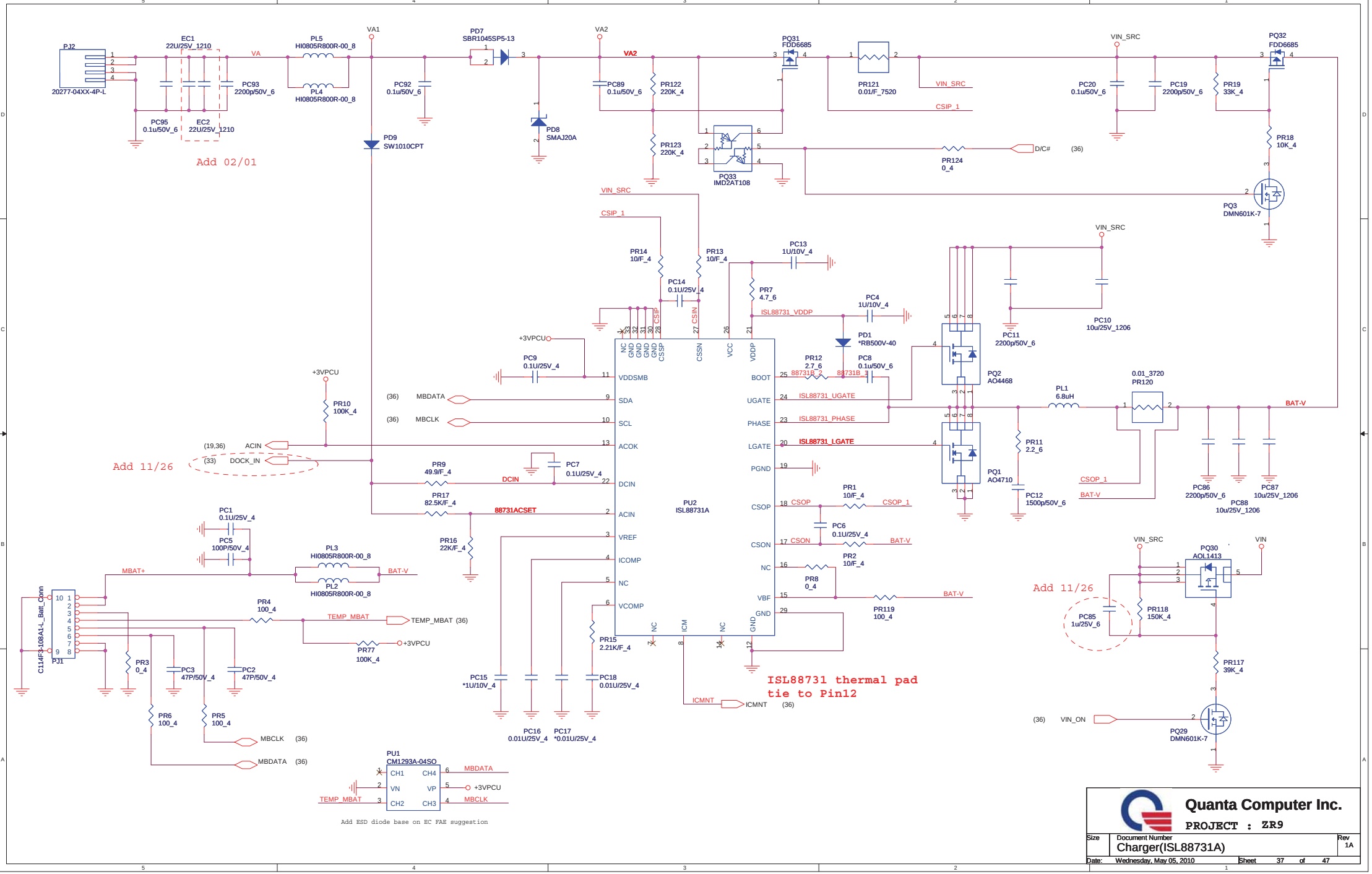
INTERNAL KEYBOARD STRIP SET

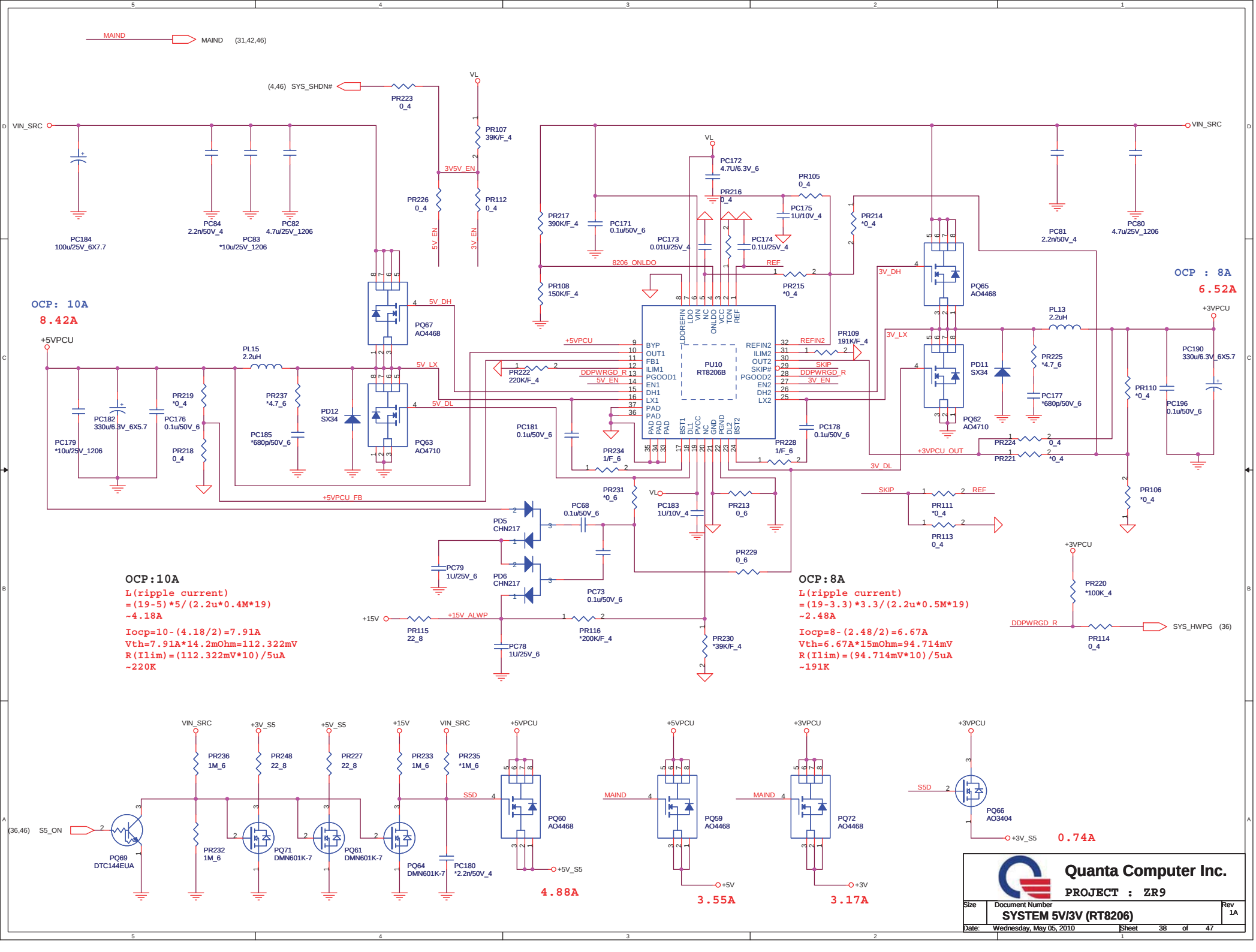
Quanta Computer Inc.

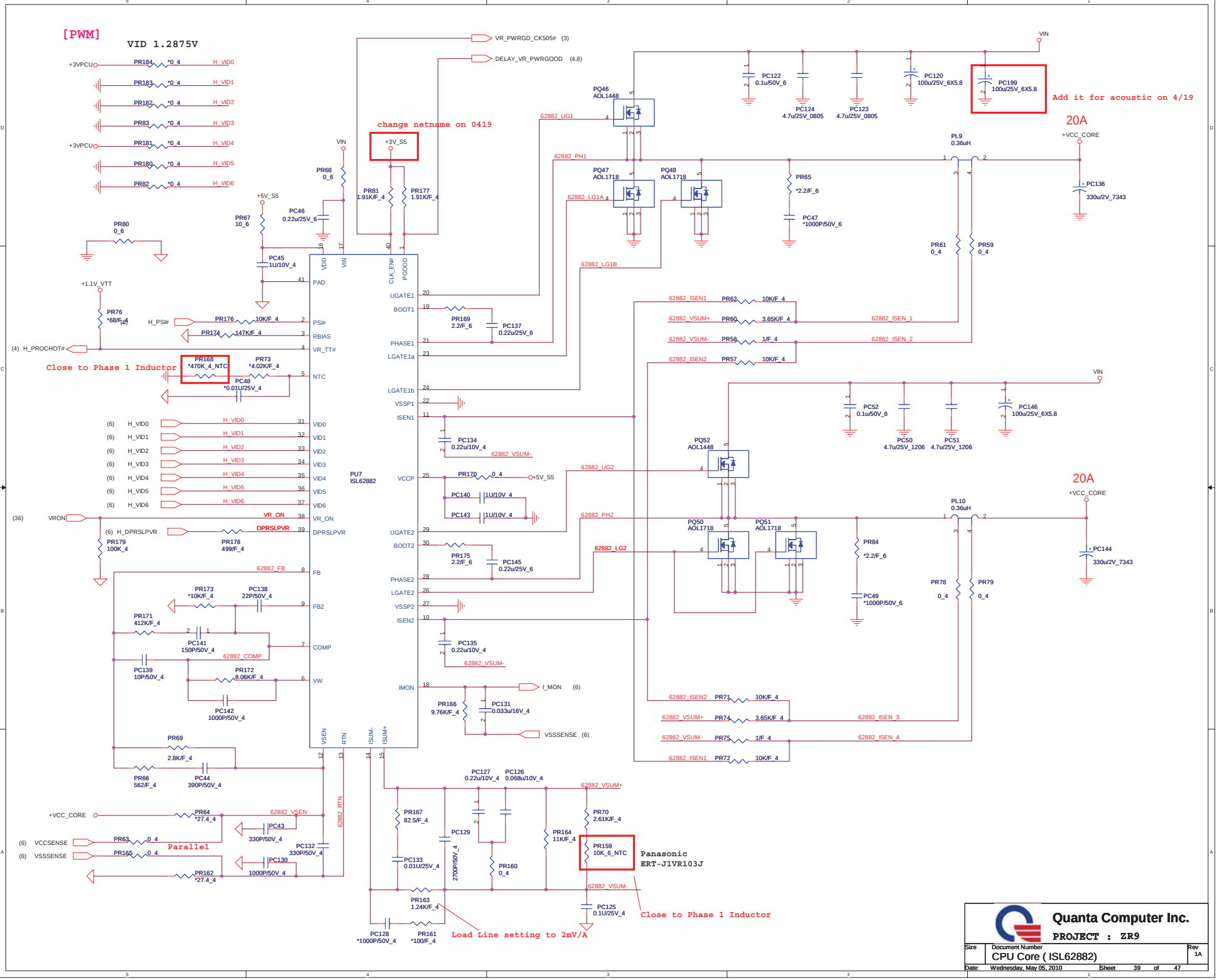
PROJECT : ZR9

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

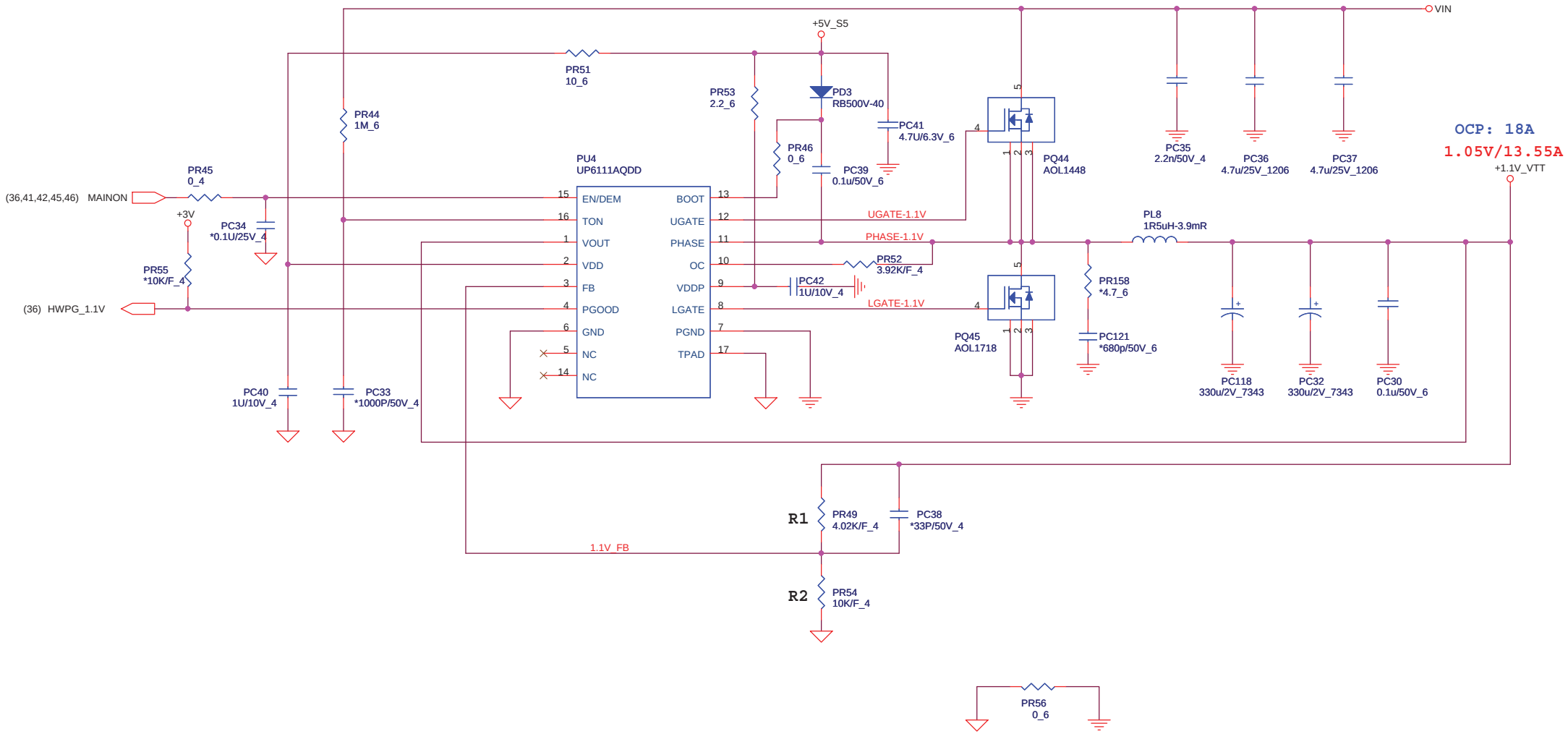
Date: Thursday, May 06, 2010 Sheet 36 of 47


PJ2
20277-04XX-4P-L
EC1
22U/25V_1210
EC2
22U/25V_1210
PC95
0.1u/50V_6
PC93
2200p/50V_6
VA
PL5
HI0805R800R-00_8
PL4
HI0805R800R-00_8
VA1
PD9
SW1010CPT
PC92
0.1u/50V_6
PD7
SBR1045SP5-13
PD8
SMAJ20A
VA2
PC89
0.1u/50V_6
PR122
220K_4
PR123
220K_4
PQ31
FDD6685
PR121
0.01/F_7520
VIN_SRC
CSIP_1
PR124
0_4
D/C#
(36)
PQ33
IMD2AT108
PC20
0.1u/50V_6
PC19
2200p/50V_6
PR19
33K_4
PQ32
FDD6685
PR18
10K_4
PQ3
DMN601K-7
Add 02/01
PR14
10/F_4
PR13
10/F_4
PC14
0.1U/25V_4
PC13
1U/10V_4
PR7
4.7_6
ISL88731_VDDP
PC4
1U/10V_4
PD1
*RB500V-40
PC8
0.1u/50V_6
PR12
2.7_6
88731B_2
88731B_1
+3VPCU
PC9
0.1U/25V_4
PR10
100K_4
(36) MBDATA
(36) MBCLK
(19,36) ACIN
(33) DOCK_IN
Add 11/26
PR9
49.9/F_4
DCIN
PC7
0.1U/25V_4
PR17
82.5K/F_4
88731ACSET
PR16
22K/F_4
PC1
0.1U/25V_4
PC5
100P/50V_4
PL3
HI0805R800R-00_8
PL2
HI0805R800R-00_8
MBAT+
BAT-V
PR4
100_4
TEMP_MBAT
TEMP_MBAT (36)
PR77
100K_4
+3VPCU
PR3
0_4
PC3
47P/50V_4
PC2
47P/50V_4
PR6
100_4
PR5
100_4
MBCLK (36)
MBDATA (36)
C114F3-108A1-L_Batt_Conn
PJ1
PU2
ISL88731A
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
NC
ICM
NC
GND
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
CSOP
CSON
PR1
10/F_4
PC6
0.1U/25V_4
PR2
10/F_4
PR8
0_4
PR119
100_4
PR15
2.21K/F_4
PC15
*1U/10V_4
PC16
0.01U/25V_4
PC17
*0.01U/25V_4
PC18
0.01U/25V_4
ICMNT
ICMNT (36)
ISL88731 thermal pad
tie to Pin12
PQ2
AO4468
PQ1
AO4710
PC11
2200p/50V_6
PC10
10u/25V_1206
PL1
6.8uH
0.01_3720
PR120
PR11
2.2_6
PC12
1500p/50V_6
PC86
2200p/50V_6
PC88
10u/25V_1206
PC87
10u/25V_1206
PQ30
AOL1413
VIN
PC85
1u/25V_6
PR118
150K_4
PR117
39K_4
(36) VIN_ON
PQ29
DMN601K-7
PU1
CM1293A-04SO
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZR9
Size
Document Number
Charger(ISL88731A)
Rev
1A
Date: Wednesday, May 05, 2010
Sheet 37 of 47


MAIND
MAIND (31,42,46)
(4,46) SYS_SHDN#
PR223 0_4
VL
PR107 39K/F_4
3V5V_EN
PR226 0_4
PR112 0_4
5V_EN
3V_EN
VIN_SRC
PC184 100u/25V_6X7.7
PC84 2.2n/50V_4
PC83 *10u/25V_1206
PC82 4.7u/25V_1206
PR217 390K/F_4
PC171 0.1u/50V_6
PC173 0.01U/25V_4
PC172 4.7U/6.3V_6
PR216 0_4
PC174 0.1U/25V_4
PR105 0_4
PC175 1U/10V_4
PR214 *0_4
PC81 2.2n/50V_4
PC80 4.7u/25V_1206
8206_ONLDO
REF
PR215 *0_4
PR108 150K/F_4
OCP: 10A
8.42A
OCP : 8A
6.52A
5V_DH
PQ67 AO4468
3V_DH
PQ65 AO4468
+5VPCU
PL15 2.2uH
5V_LX
3V_LX
PL13 2.2uH
+3VPCU
PR222 220K/F_4
DDPWRGD_R
5V_EN
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
PU10 RT8206B
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
BST1
DL1
PVCC
NC
GND
PGND
DL2
BST2
REFIN2
PR109 191K/F_4
SKIP
DDPWRGD_R
3V_EN
PD11 SX34
PR225 *4.7_6
PC177 *680p/50V_6
PC190 330u/6.3V_6X5.7
PC196 0.1u/50V_6
PR110 *0_4
PR219 *0_4
PR237 *4.7_6
PD12 SX34
5V_DL
PC182 330u/6.3V_6X5.7
PC176 0.1u/50V_6
PC179 *10u/25V_1206
PR218 0_4
PC185 *680p/50V_6
PQ63 AO4710
PC181 0.1u/50V_6
PR234 1/F_6
PC178 0.1u/50V_6
PR228 1/F_6
PQ62 AO4710
PR224 0_4
PR221 *0_4
+3VPCU_OUT
3V_DL
+5VPCU_FB
PR231 *0_6
PC68 0.1u/50V_6
PC183 1U/10V_4
PR213 0_6
SKIP
REF
PR111 *0_4
PR113 0_4
PR106 *0_4
PD5 CHN217
PD6 CHN217
PC79 1U/25V_6
PC73 0.1u/50V_6
PR229 0_6
+3VPCU
PR220 *100K_4
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
+15V
PR115 22_8
+15V_ALWP
PR116 *200K/F_4
PC78 1U/25V_6
PR230 *39K/F_4
DDPWRGD_R
PR114 0_4
SYS_HWPG (36)
VIN_SRC
+3V_S5
+5V_S5
+15V
VIN_SRC
+5VPCU
PR236 1M_6
PR248 22_8
PR227 22_8
PR233 1M_6
PR235 *1M_6
S5D
PQ60 AO4468
(36,46) S5_ON
PQ69 DTC144EUA
PR232 1M_6
PQ71 DMN601K-7
PQ61 DMN601K-7
PQ64 DMN601K-7
PC180 *2.2n/50V_4
+5V_S5
4.88A
+5VPCU
MAIND
PQ59 AO4468
+5V
3.55A
+3VPCU
MAIND
PQ72 AO4468
+3V
3.17A
+3VPCU
S5D
PQ66 AO3404
+3V_S5
0.74A
Quanta Computer Inc.
PROJECT : ZR9
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Wednesday, May 05, 2010
Sheet 38 of 47


[PWM]
VID 1.2875V
+3VPCU
PR184 *0_4 H_VID0
PR183 *0_4 H_VID1
PR182 *0_4 H_VID2
PR83 *0_4 H_VID3
PR181 *0_4 H_VID4
PR180 *0_4 H_VID5
PR82 *0_4 H_VID6
VR_PWRGD_CK505# (3)
DELAY_VR_PWRGOOD (4,8)
change netname on 0419
+3V_S5
VIN
PR68 0_6
PR81 1.91K/F_4
PR177 1.91K/F_4
PC46 0.22u/25V_6
+5V_S5
PR67 10_6
PR80 0_6
PC45 1U/10V_4
+1.1V_VTT
PR76 *68/F_4
H_PSI#
PR176 10K/F_4
PR174 147K/F_4
(4) H_PROCHOT#
Close to Phase 1 Inductor
PR168 *470K_4_NTC
PR73 *4.02K/F_4
PC48 *0.01U/25V_4
(6) H_VID0
(6) H_VID1
(6) H_VID2
(6) H_VID3
(6) H_VID4
(6) H_VID5
(6) H_VID6
(36) VRON
VR_ON
(6) H_DPRSLPVR
DPRSLPVR
PR179 100K_4
PR178 499/F_4
PU7 ISL62882
VDD
VIN
CLK_EN#
PGOOD
PAD
UGATE1
BOOT1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1
VCCP
UGATE2
BOOT2
PHASE2
LGATE2
VSSP2
ISEN2
IMON
PSI#
RBIAS
VR_TT#
NTC
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
FB
FB2
COMP
VW
VSEN
RTN
ISUM-
ISUM+
62882_FB
PR173 *10K/F_4
PC138 22P/50V_4
PR171 412K/F_4
PC141 150P/50V_4
62882_COMP
PC139 10P/50V_4
PR172 8.06K/F_4
PC142 1000P/50V_4
PR69 2.8K/F_4
PR66 562/F_4
PC44 390P/50V_4
PR169 2.2/F_6
PC137 0.22u/25V_6
PC134 0.22u/10V_4
62882_VSUM-
PR170 0_4
+5V_S5
PC140 1U/10V_4
PC143 1U/10V_4
PR175 2.2/F_6
PC145 0.22u/25V_6
PC135 0.22u/10V_4
62882_VSUM-
PR166 9.76K/F_4
PC131 0.033u/16V_4
I_MON (6)
VSSSENSE (6)
62882_UG1
62882_PH1
62882_LG1A
62882_LG1B
62882_UG2
62882_PH2
62882_LG2
PQ46 AOL1448
PQ47 AOL1718
PQ48 AOL1718
PQ52 AOL1448
PQ50 AOL1718
PQ51 AOL1718
PC122 0.1u/50V_6
PC124 4.7u/25V_0805
PC123 4.7u/25V_0805
PC120 100u/25V_6X5.8
PC199 100u/25V_6X5.8
Add it for acoustic on 4/19
20A
PL9 0.36uH
+VCC_CORE
PC136 330u/2V_7343
PR65 *2.2/F_6
PC47 *1000P/50V_6
PR61 0_4
PR59 0_4
62882_ISEN1 PR62 10K/F_4
62882_VSUM+ PR60 3.65K/F_4
62882_ISEN_1
62882_VSUM- PR58 1/F_4
62882_ISEN_2
62882_ISEN2 PR57 10K/F_4
PC52 0.1u/50V_6
PC50 4.7u/25V_1206
PC51 4.7u/25V_1206
PC146 100u/25V_6X5.8
20A
PL10 0.36uH
+VCC_CORE
PC144 330u/2V_7343
PR84 *2.2/F_6
PC49 *1000P/50V_6
PR78 0_4
PR79 0_4
62882_ISEN2 PR71 10K/F_4
62882_VSUM+ PR74 3.65K/F_4
62882_ISEN_3
62882_VSUM- PR75 1/F_4
62882_ISEN_4
62882_ISEN1 PR72 10K/F_4
+VCC_CORE
PR64 *27.4_4
62882_VSEN
PC43 330P/50V_4
(6) VCCSENSE
PR63 0_4
Parallel
(6) VSSSENSE
PR165 0_4
PC130 1000P/50V_4
PR162 *27.4_4
PC132 330P/50V_4
62882_RTN
PC127 0.22u/10V_4
PC126 0.068u/10V_4
62882_VSUM+
PR167 82.5/F_4
PC129 2700P/50V_4
PR164 11K/F_4
PR70 2.61K/F_4
PR159 10K_6_NTC
Panasonic
ERT-J1VR103J
PC133 0.01U/25V_4
PR160 0_4
62882_VSUM-
PR163 1.24K/F_4
PC125 0.1U/25V_4
Close to Phase 1 Inductor
PC128 *1000P/50V_4
PR161 *100/F_4
Load Line setting to 2mV/A
Quanta Computer Inc.
PROJECT : ZR9
Size
Document Number
CPU Core (ISL62882)
Rev 1A
Date: Wednesday, May 05, 2010
Sheet 39 of 47

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

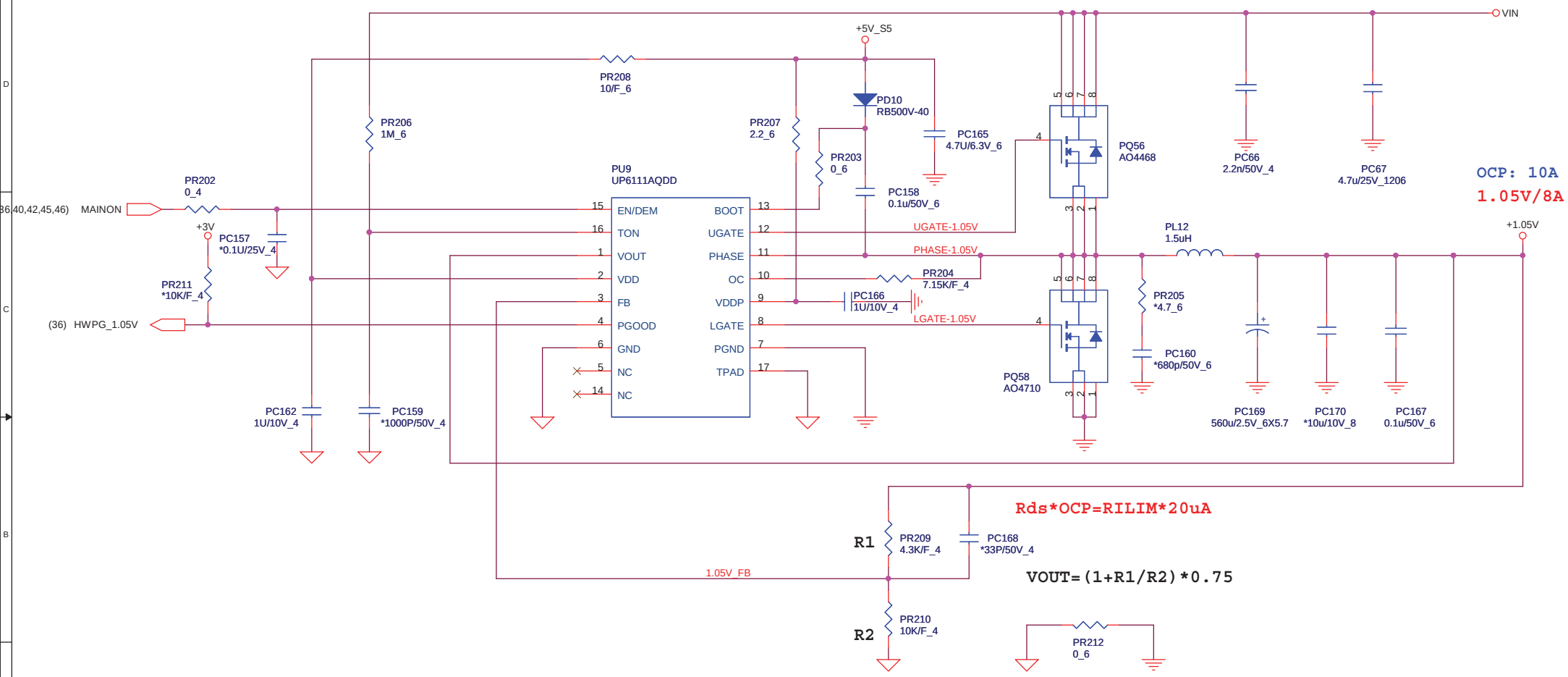
Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: +VTT (UP6111A)	Rev 1A
Date: Wednesday, May 05, 2010	Sheet 40 of 47	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1.5u*272k*19)
~2.431A

14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K

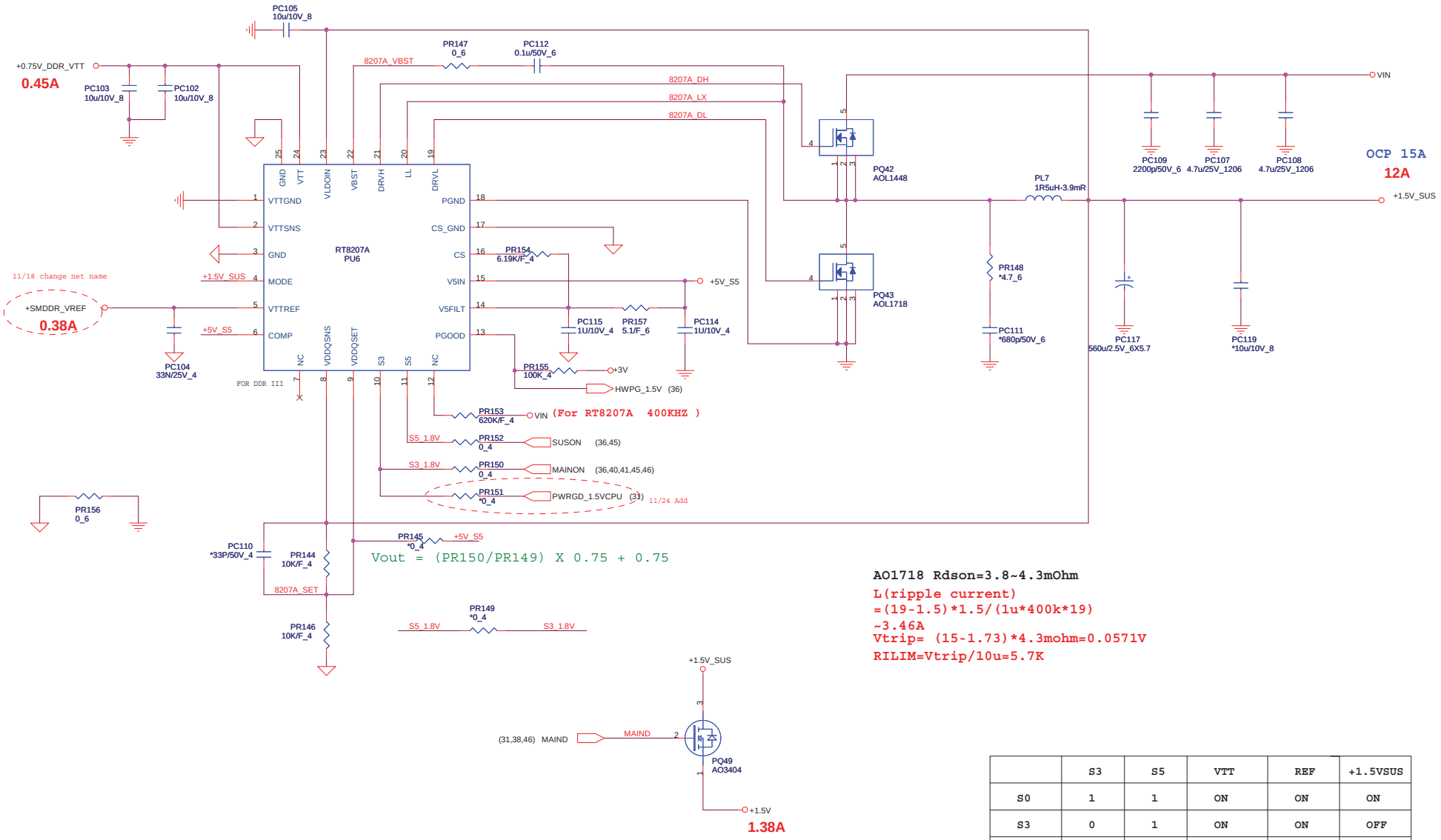
Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A

Date: Wednesday, May 05, 2010 Sheet 41 of 47

[PWM]



Vout = (PR150/PR149) X 0.75 + 0.75

AO1718 Rdson=3.8~4.3mOhm

L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.46A
Vtrip= (15-1.73)*4.3mohm=0.0571V
RILIM=Vtrip/10u=5.7K

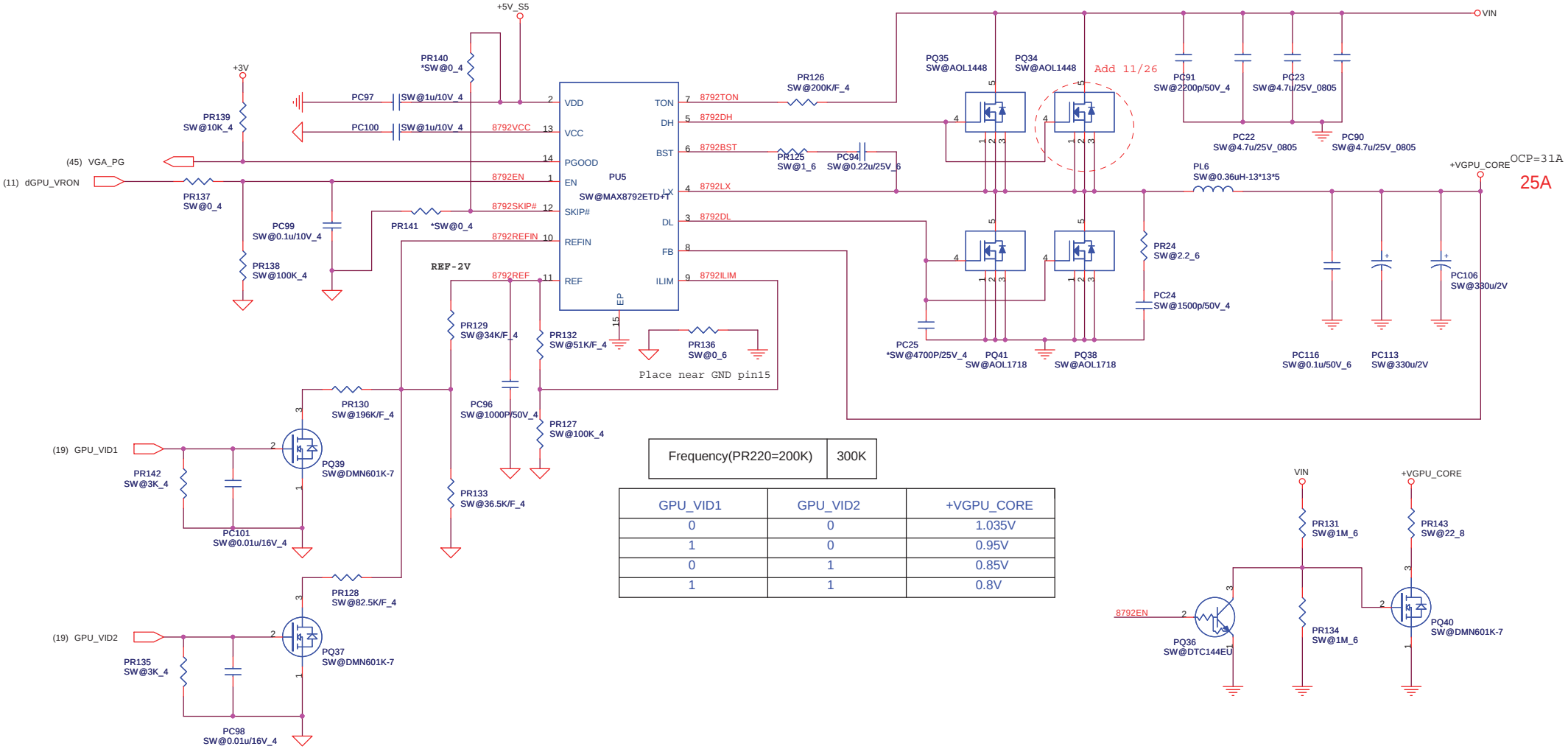
	S3	S5	VTT	REF	+1.5VSUS
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Wednesday, May 05, 2010 Sheet 42 of 47



Frequency(PR220=200K)	300K

GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	1.035V
1	0	0.95V
0	1	0.85V
1	1	0.8V

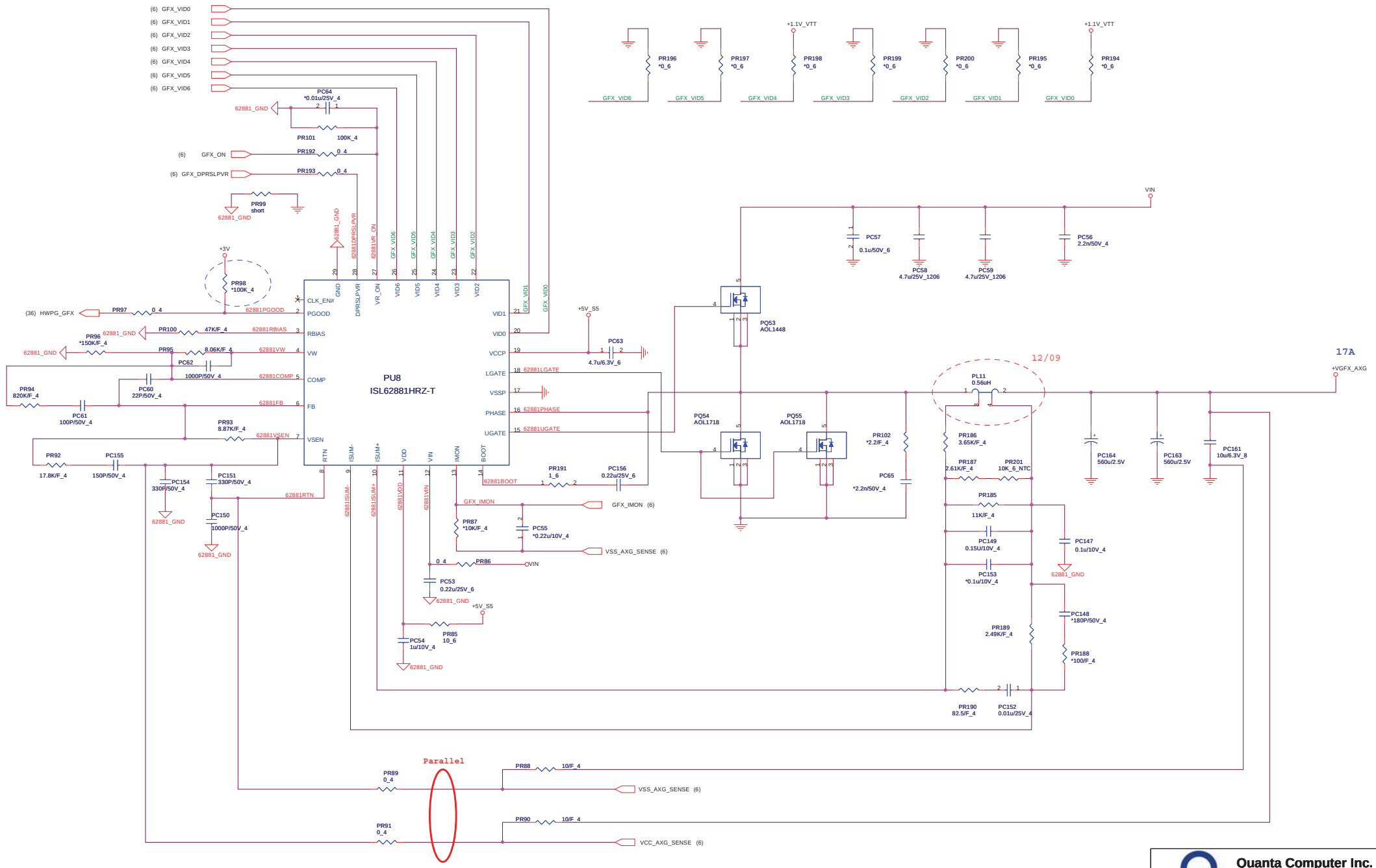
Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A

Date: Thursday, April 29, 2010 Sheet 43 of 47

Int_VGA [PWM]



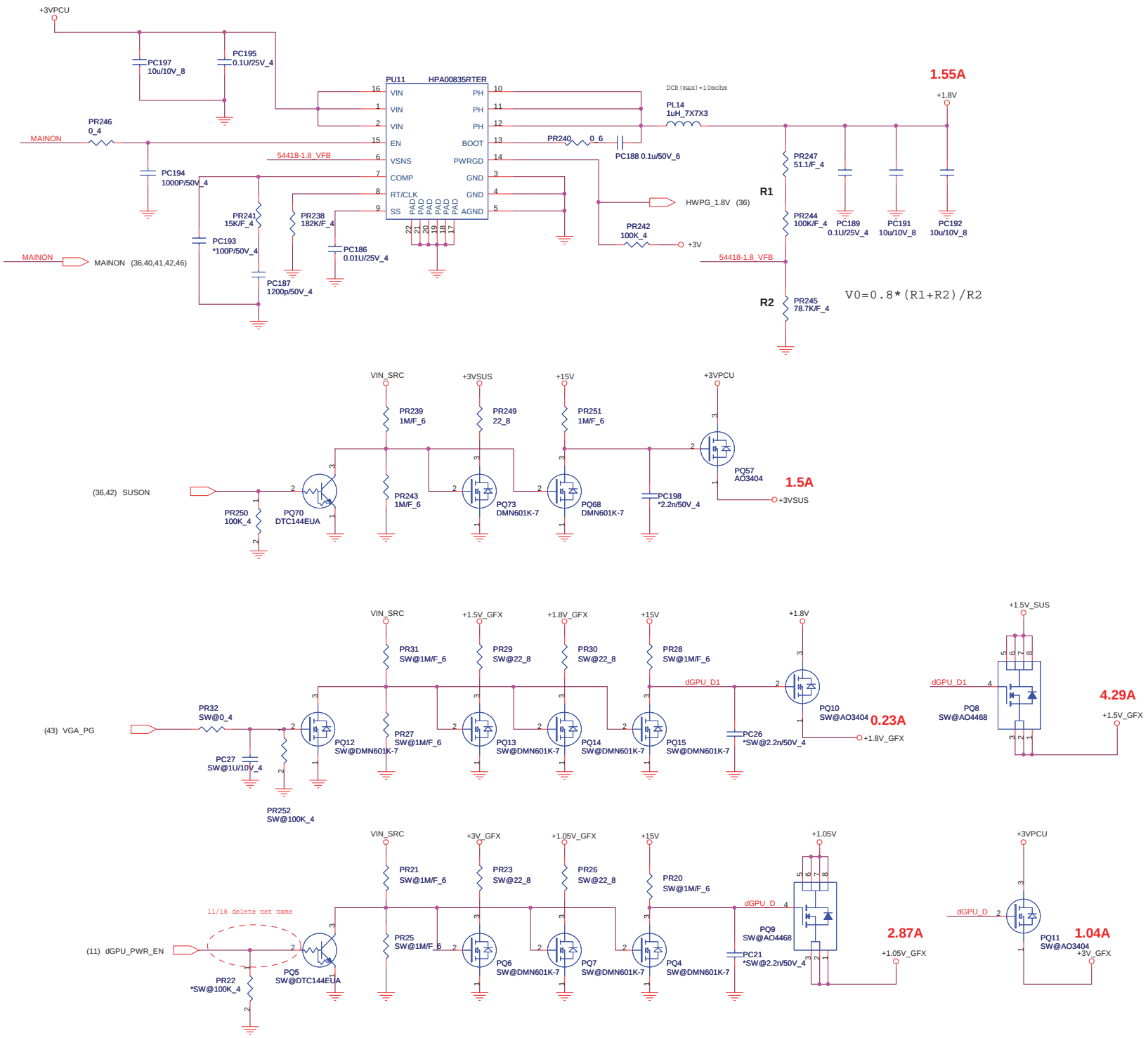
Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A

Date: Wednesday, May 05, 2010 Sheet 44 of 47

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

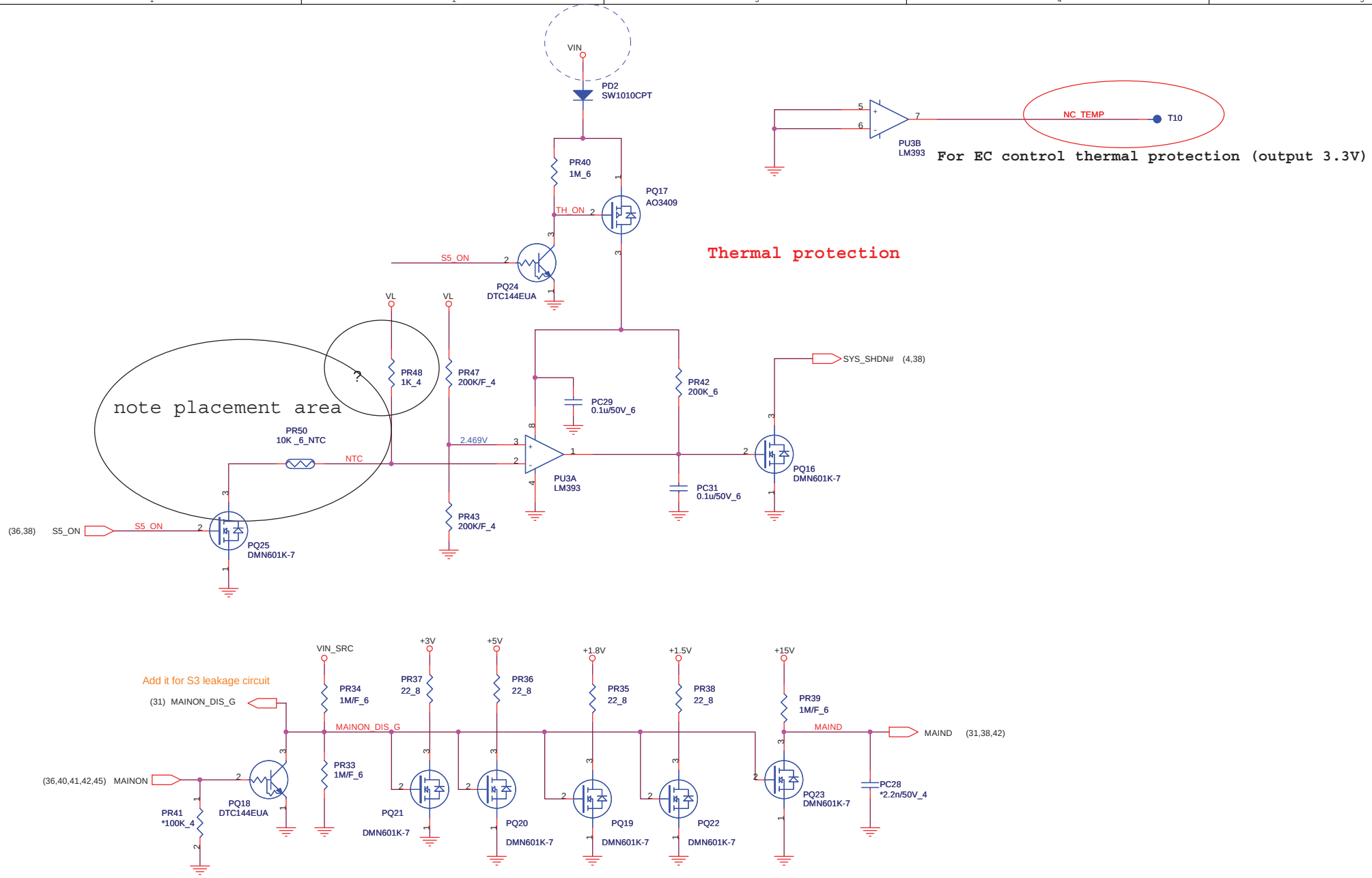


Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	(GPU_Power/1.8V)	1A

Date: Wednesday, May 05, 2010 Sheet 45 of 47



Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	Thermal Protection	1A

Date: Wednesday, May 05, 2010 Sheet 46 of 47

CHANGE LIST

Model	REV	DATE	CHANGE LIST
ZR9	A	20091117	page 10:delete R8345 & add C8407 & modify usb port define --> sim card to port 5 ,docking to port 0
			page 34:modify CN7009 pin define
			page 30:modify speaker out circuit
			Evan Wang update Power circuit
		20091119	page 33 :cn9055 pin.67 change net name DCIN to DOCK_IN
			page 18 Base on Design guide , DVI should change to port E.
			Evan Wang update Power circuit
		20091124	page 4 :add R529,R232,R537,R527,R213,R524,R538,R536,R534,R528,R230
			page 19 :delete R3515,R3514,Q3500,Q3501
			page 24 :change net name MB_HDMI_DDCDATA ,MB_HDMI_DDCCLK to SDVO_CTRL_DAT, DVO_CTRL_CLK
			page 34 :delete R7451 & change R7442 to 1K , add C8031,C9053
		20091125	page 30 :U9001 Pin.26 C12021change PD to AGND & add R13069,R228,R233
			page 24 :delete R9798,R9810
			page 35 :add LED7005,R7402,R7408 & modify CN7008 Pin define
			page 19 :add R3590 to PU +3V_GPX
		20091126	Evan Wang update Power circuit 1. Add PC9020(1u/25V_6),2. PR9028 changes to 150K_4,3. PR9025 changes to 39K_4,4. Add PQ3008(SW@AOL1448),5.GPU CORE solution change to MAX8752.
			page 35 :del LED7005,R7402,R7408
		20091127	page 14 :JDIM8000 SWAP PIN
			page 15 :JDIM8999 SWAP PIN
			page 21 :U3502,U3509,U3503,U3508 SWAP PIN
			page 22 :U3504,U3500,U3501,U3507 SWAP PIN
			page 24 :U15 SWAP PIN
			page 27 :U45 SWAP PIN
			page 32 :delete R295,R296,R297,R298,R363,R346,L28,L29,L32
		20091130	page 16 :delete C3513,C3500,C3643,C3644,C3501
			page 21 :delete C557,C559,C7,C560
			page 22 :delete C565,C563,C20,C564
			page 35 :add LED2,R7402 & modify CN7008 Pin define
			page 23 :CN9049 modify pin define & change 6 pin
		20091201	page 32 :CN7008 modify pin define
			page 36 :U7020.14 net name WLN_LED# change to U7020.112 & add net name WL_LED# on U7020.98
			Evan Wang update Power circuit
		20091202	page 6 :del R8237
			page 12:del R8268 & add R8432,R8433
			page 30:del R228
		20091203	page 32:CN11 change Pin define
			page 35:del D13,D7022 & add R13093,R12101
		20091207	page 35:add R7406,LED7001
			page 23:CN9049 change to 8 pin
		20091210	page 35:R7398,R7399,R7400R7402,R7403,R7404,R7405,R7406 chnage to 150 ohm
		20091214	page 35:add Q7027
			page 24:add R9802,R9795
	B	20100106	page 4: change R185 to NC
			page 8: change R395 to un-mount
		20100125	page 10: change C715,C714 to 33pf & add R508,R653,R654,R655,R656,R657 & for LAN SMBus form SMB_CLK_ME0,SMB_DATA_ME0 to ICH_SMBCLK,ICH_SMBDATA & change high resistor 4.7k ohm R134,R135 close to chip side
			page 11: chnage dGPU_PWR_EN pin high resistor IV@ un-mount
			page 18: change C595,C596 to 33pf
			page 23: VGA power add poly switch
			page 26: LAN SMBus change net name to ICH_SMBCLK,ICH_SMBDATA & C228,C229 to 33pf
			page 28: del net name RF_EN & R559 & R511 un-mount
			page 31: change R508 to NC
			page 33: DOCK power add poly switch & R269,C392 un-mount
			page 35: change Q9 to N type & add R660,R659
			page 36: add R658
			Evan Wang update Power circuit
		20100127	page 30: add connector CN25 & change L29 , L30 , L31 , L32 , L47, L48 , C531 , C530 to docking side
			page 33: add connector CN26
			page 33: CN17 ADOGND change to ADOGND_2
		20100201	Evan Wang update Power circuit
			page 23: add U51
		20100202	page 33: CN26 ADOGND change to ADOGND_2
			page 36: add R547
			page 33: add R554,R559 & D27
		20100205	page 33: Docking power add f2,f3
			page 27: CN12 chnage footprint
	C	20100325	page 12: Add C530 to decrease CRT DAC ripple noise
			page 25: Change R589, R592 to bead for EMI require
			page 30: C478, C500 change from Y5V to X7R for MIC THD+N quality
			page 30: R404 pull high R to 100K for docking insert detect
			page 35: Change POWLED# power to +3V_S5 to prevent when EC go into power saving, power LED will turn on in battery only.
			page 35: Modify 3G/WIFI LED turn on behavior.
	Ramp	20100416	page 32 : Modify B/T power from +3V to +3V_S5
			page 23 , 1. Change L1 to 0805 size 2. Change R12 , R13 from 0603 to 0402
			page 31 : Change PR103 , PQ27 to N.C
			page 23 , 36 : Delete PANEL_COLOR and PANEL_ENG per EC required.
			page 41 : PR209 changes to 4.3K/F_4(CS24302PB07)
			page 37 : Mount PR11 and changes to 2.2_6(CS-2203P911)
			page 37 : Mount PC12 and changes to 1500p/50V_6(CH21506K915)
			page 43 : PR24 changes to SW@2.2_6(CS-2203P911)
			page 43 : PC24 changes to SW@1500p/50V_4(CH21506KB14)
			page 35 : Change BXP power LED size from 0805 to 0603 and the quantity increase to two
			page 23 : Add cap. C531 , C748-C752 for monitor test
		20100420	page 23 : Remove R12 , R13 and mount common mode choke L1 for EMI requirement
			page 25 : R589,R592 need to mount the bead SBY100505T121YN(CX05T121000) for EMI requirement
			page 30 : EMI suggested that R421 , R331 need to be mounted
			page 30 : R384 , R385 need to mount the bead(CX47T10000) for EMI
			page 30 : C525 , C527 need to mount cap. 20pF for EMI

Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	Change List01	1A

Date: Thursday, May 06, 2010 Sheet 47 of 47